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Test Scheduling of SoC by using Dynamic Voltage Frequency Scaling (DVFS) Technique

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Abstract: High temperature gradients in System on Chip (SoC) lowered the performances, reliability and leakage power. In addition, temperature during testing gain more compared to normal operation. Therefore, the investigation of the impact dynamic voltage frequency scaling (DVFS) on the thermal aware test scheduling performance will be the main contribution of this work. The test scheduling algorithm which embeds frequency scaling effect with dynamic voltage supply is tested on ITC'02 benchmark. The formulation of ILP is to minimize the group of the test session in SoC and continued with DVFS formulation. Compared to the conventional thermal-aware scheduling approach based purely on a frequency scaling, this technique provides shorter overall test times and greatly improved flexibility to satisfy strict thermal constraints. The proposed DVFS with thermal aware task scheduling allows to minimize test time more than 46%.

Keywords: DVFS, thermal, frequency scaling and test time

1. Introduction

For modern VLSI technology it shows the overheating during testing during very serious problems due to rising power consumption, thus increasing the chip temperature. Working at high temperatures will cause the transistors to fail to switch properly, and many failure mechanisms, such as electro-migration, are accelerated, resulting in reliability or even permanent damage decreasing overall. These problems are exacerbated for core-based system-on-chip (SOC) designs because, quite often, several embedded cores are tested concurrently in order to reduce the overall test time. There has been cover over the past decade on low power devices and energy consumption has become one of the major criteria for these devices [1]. Circuit techniques for low voltage operation techniques and also standby current reduction with optimal gate sizing have also been explored and are available for use by a designer [2]. This low power issue was extending to temperature problem. In the recent year, DVFS management techniques have emerged with thermal aware, where the DVFS is continuously adjusted during test time of the SoC [1, 3-6]. The maximum temperature needs to be controlled beyond a certain threshold during thermal aware between DVFS and test partition technique.

It is inspired by the fact that because, in most optimistic scenarios, the SoC is designed to satisfy the most challenging device throughput needs, it contributes to an excess power variance in normal operating conditions. DVFS technique used in this paper to resolve the problem and determine the effect on the thermal aware test scheduling. In Section 2, review some commonly used techniques in thermal aware scheduling and DVFS. In Section 3, the formulation to determine frequency and voltage for each test session is presented. This is to improve hotspot free and minimize the testing time under thermal constraints. The experimental validation of the proposed approach is discussed in Section 4.

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2. Related Works

Recently most of the papers highlight the problem of temperature in test scheduling have been published [6-13]. The first group of researchers cover thermal aware test scheduling was Rosinger et al. in [13] which captures the temperature at granularity level by utilizing the adjacency information in RC formula in order to have the best test scheduling. The heat flow, thermal resistance and thermal capacitance in the RC thermal model are identical to the electrical current, electrical resistance, and electrical capacitance, respectively. In addition, and the electrical voltage is presented by the difference temperature. However, during the test scheduling they used the fixed frequency and also ignore the effect of metal interconnect as one of the heat conductors and one of the critical layers that spreads over the die due to the increased functionality if the IC. In paper [7], the authors proposed an optimal mixed integer linear programming and also seed based clustering heuristic in order to get the best test scheduling with thermal constraints. However, this technique only applicable to static thermal profile due to difficulty to estimate the temperature during transient and attach with this idea. The authors of [9] describe the problem as a rectangle packaging heuristic and partition the test scheduling to prevent core under test from reach temperature limit. Nevertheless, this optimization method did not consider the power effect of heating up of each testing after stop for while (cooling period) and also ignore the neighboring core effect in thermal aware estimation.

Yao et al. [11] proposed a test partition-based thermal-aware test scheduling technique and proved that test access time can be reduced by dividing certain test into partitions. They also proposed the superposition method to calculate the thermal profiles which exploit the linear property of thermal RC model to be used in test scheduling thermal aware [12]. On other hand, this technique only offers to steady state thermal analysis and ignored the heat transfer among the cores that can generate more temperature effect. Continuously, they also ignore about frequency effect during the scheduling. He et al. concludes that a power intensive and long test violates the temperature restriction even when operating alone [9]. The approach to deal with these un-schedulable thermal tests often includes splitting the test into many short partitions that can be scheduled under the thermal constraint. The temperature of the system under test can be reduced by inserting cooling times between two partitions. This technique also ignores about heat transfer by neighboring cores and metal interconnect in temperature estimation. During test scheduling, the frequency changes effect they not consider at all.

DVFS has been used to reduce energy and power consumption during operation at system level. Most of the existing work in this field focused on deadline constrained applications with finite schedule lengths. In [6], Malican et al. proposed a test partitioning method specifically designed for thermally restricted tests to reduce the time of the 3D stacked integrated circuits under temperature constraints. However, these ideas are to complex and the data shows more partitions create more opportunity for test overlap even not always. Recently, Li Ling et al. [4] proposed DVFS techniques for thermal aware with constant power dissipation during test. However, during the test power and temperature will experience the variations. Therefore, power interval must be considered in test scheduling. For the SoC, the amount of frequency scaling depends on each power management condition. Instances where the resource consumption increases over time can increase the frequency of at least one clock. A supply voltage for circuits that use the clock may be increased prior to the frequency of the clock being increased. Similarly, in cases where there is a decrease in resource utilization over time, the frequency of the clock may be decreased. A supply voltage for circuits that use the clock may be decreased after decreasing the frequency of the clock. In particular, the relation between energy consumption and frequency is vertex. The energy consumption increases dramatically faster when frequency is high, thus when scaling down the operating frequency of a task, the majority of energy savings are done through the initial stages of scaling down frequency. However, this idea did not show the formulation clearly regarding their methods.

Several approaches have been proposed test scheduling technique using ILP for optimization. Chakrabarty [17] suggested ILP for the assignment of test bus width and the effect on test time for systems using different design. In [18], the resource constraint among each test is represented by test-compatibility-graph (TCG); the scheduling problem is formed using ILP model. Nourani and Chin [19] introduce a solution based on Mixed Integer Linear Programming (MILP) to perform power-time trade-off analyzes for SoC test schedules, allowing for a choice between several constraints including average and peak power consumption [12]. Iyengar and Chakrabarty present a scheduling technique for SoC experiments under precedent test relationships and peak power constraints [20]. An optimal MILP formulation designed for the problem of MPSoC test scheduling to manage test scenarios in which temperature is a concern. This formulation minimizes test schedule times in the presence of resource conflicts under a peak temperature constraint. In DVFS, ILP is used by manipulating the V_{dd} these constraints can be so altered such the clock frequency may be further increased, thus, minimizing the test time. Venkataramani et al. [21] addressed two test speed constraints, namely the power constraint when the test clock speed is constrained by the power output and the layout constraint when the test clock speed is restricted by the critical path or other considerations of the time. In [24], demonstrate for the first time a malicious use of the frequency regulator against a TrustZone-enabled SoC and use frequency scaling to create a covert channel in a TrustZone-enabled heterogeneous SoC.

3. Temperature Aware Dynamic Voltage Frequency Scaling (DVFS) Formulation

One of the methods that used to handle heat generation in a chip during test scheduling is Dynamic Voltage and Frequency Scaling (DVFS). This section formulates the proposed thermal safe test scheduling problem equipped with DVFS technique using Integer Linear Programming (ILP) in order to have shorter test application time (TAT). The test compatibility graph (TCG) provides information of cores which can be tested concurrently in the system. The goal of ILP is to minimize a linear objective function on a set of integer and variables that formulates test time, while satisfying a set of linear constraints including temperature limit and resource constraints. ILP produces the best test session which meets all the constraints. ILP for test scheduling is established using MATLAB. Thermal simulator is invoked during test time optimization process and DVFS is performed. The proposed test scheduling is based on the concept of test sessions. Specifically, the test time for SoC is determined by the selected test sessions, where each core is associated with one test session. A group of test sessions are executed in series. The shortest test schedule can be determined by manipulating the voltage supply and frequency of the system using DVFS.

Therefore, in DVFS, the system is able to scale up and scale down the frequency based on the requirement. During scaling up, the test clock rate will produce more power consumption; thus, it exacerbates the temperature effect. Thus, scaling up the frequency needs to be constrained by temperature limit, T_{max}. Constrained by T_{max} alone is not sufficient because too high frequency which requires clock period shorter than one allowable by the core's critical path violates design rules (structural constraint) and will cause incorrect functioning. To make the maximum frequency a valid frequency, optimal voltage value that allows test to be performed at maximum frequency without exceeding T_{max} of the device and without violating structural constraint.

In this work, the operating voltage range is expected to range from 0.6V (minimum) to 1.0V (minimal). To find optimum voltage, V_{ddopt}, for each iteration the value of the V_{dd} is varied from 1.0V to 0.6V with a decrease of 0.1V. A core's test power depends on the voltage. The supply voltage also affects the structural and power constraints which restrict the highest frequency of a core. The power consumption, P changes with V_{dd} and clock frequency, f as in Equation (1).

$$P \propto {V_{dd}}^2 . f \qquad (1)$$

This equation shows the power consumption can be reduced by lowering operating voltage. However, by reducing the operating voltage, the test time will increase. Therefore, it is required to find an optimum V_{dd} and frequency that allows balancing the tradeoffs at the same time, achieves time reduction.

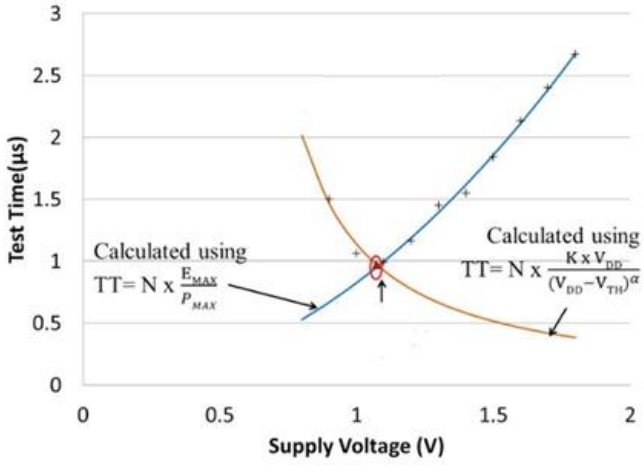

Fig. 1 - Test Time Vs V_{dd} on optimal condition

As seen from the above expression in Fig. 1, reducing the voltage causes the delay to increase, which in turn, slows down the execution testing. TT1 is derived based on power limit for testing whereas TT is derived based on critical path delay. On one hand, reducing V_{dd} lowers power consumption allows higher clock rates thereby shrinking to shorten the total test time. On the other hand, the increased circuit delay results in slower clock rate and a longer test time. Therefore, each core is limited with power constrained frequency limit, f_p and structurally constrained frequency limit, f_s. Red circle in this graph is an optimal time and optimum V_{dd}.

The changes on voltage supply, V_{dd}, will change the power accordingly. Changes on V_{dd} also affect f_p and f_s based on Equation (2) and Equation (3). The power rating for a core is constant; so, the relation f_p-V_{dd} can be expressed as:

$$f = \frac{1}{{V_{dd}}^2} \qquad (2)$$

The alpha power law defines the relationship between f_s-V_{dd} as:

$$f \propto \frac{(V_{dd} - V_{th}))^2}{V_{dd}} \qquad (3)$$

Then, rewrite the Equation (2) and Equation (3) to Equation (4) and Equation (5) where C_1 and C_2 are constants.

$$f_p \propto \frac{1}{{V_{dd}}^2} = C_1 \frac{1}{{V_{dd}}^2} \qquad (4)$$

$$f \propto \frac{(V_{dd} - V_{th}))^2}{V_{dd}} = C_2 \frac{(V_{dd} - V_{th}))^2}{V_{dd}} \qquad (5)$$

Since every core is provided with f_s and f_p, values of f_p and f_s are selected from a core in the session such that they are lowest frequency in the session. The values of f_p and f_s are important to find an optimum valid frequency for the session. Given a value of V_{dd} for a core, the lower frequency is chosen between the selected f_s and f_p such that the operation of the cores in the session violates neither structural constraint nor test power constraint. Based on the selected V_{dd} value for each session, the new power is calculated based on Equation (1) which can now be written as Equation (6):

$$P \propto {V_{dd}}^2 . f_p \qquad (6)$$

Another factor that determines how much frequency can be scaled is the ratio of maximum power, P_{max} to session power, $P_{session}$. The power ratio indicates how many times a frequency can be scaled up/down before the resulting power reach P_{max}. The frequency factor, F_m is formulated to determine the how much scaling up/down frequency is allowed as stated in Equation (7):

$$F_m = \min\left(\frac{min\{f_p, f_s\}}{f_o}, \frac{P_{max}}{P_{session}}\right) \qquad (7)$$

where f_o is the frequency of the slowest core. There are many cores in a test session whose original frequency may be different from each other. During testing without DVFS, only one frequency will be used, so the slowest frequency, f_o will be used as testing speed to avoid structural constraint violation in other cores in the same session. That's the reason why f_o is based in calculating F_m.

Later, thermal simulation is performed based on the new power generated using scaling voltage. After that, total cost of test scheduling is determined by the total test time. This total cost is determined by the summation of test time of each session. If a temperature of test session has still not reached the limit and V_{dd} is below than 0.6V, the voltage will be reduced for another 0.1V and repeating until the limit with the last test time and temperature value recorded The DVFS technique is heuristic because V_{dd} reduction of 0.1V and temperatures of a session are used to decide whether the session's frequency is reaching the maximum or not. The heuristic algorithm starts by checking whether an individual core complies with the maximum allowable temperature limit, T_{max}. The decision to determine either the frequency of that session should be increased further or not depends on temperature of that session. If the temperature of the session is lower than temperature limit, the session has chance to be scaled up. However, if the temperature of the session is more than temperature limit, the maximum frequency will be used.

Value of V_{dd} start from nominal voltage, and reduce 0.1V in each iteration. For each iteration, the algorithm computes the core's frequency constraints (f_s and f_p), test power and temperature. Based on these values, the frequency factor, F_m is updated. The overall test time is computed. If the test time has reduced, it implies that the test may not yet reach optimum condition. The above steps are repeated again. If the test time has increased due to V_{dd} reduction, it implies the test time transitioned unto structure constrained domains and it stops the voltage scaling down procedure.

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4. DVFS Results

In order to determine the accuracy of DVFS technique on SoC benchmark circuit, the comparison has been made between our proposed session-based test scheduling with DVFS technique and session-based test scheduling without DVFS [23]. Second comparison has been done to work [4]. Both of these techniques implement thermal constraint in the scheduling algorithm in order to generate test schedule.

Table 1 compares the test time and temperature of each test session for five benchmarks circuits. As could be observed from the given data, the test sessions for both techniques are the same. This is because ILP technique is used for both to define test sessions using the same set of constraints. For every test session, power consumption only dissipates for active cores only while other cores are assumed to be grounded. For d695, with 10 cores, 3 test sessions are required to complete the test. However, even the number of cores for a586710 is 6; only one session is required to be tested. Thus, this affected the simulation time which is much faster compared to SoC with many sessions. The temperature values for our proposed technique are provided in Column 3 and for test session-based test scheduling technique without DVFS the temperature values are shown in Column 7. Generally, the observation shows that the proposed technique produced much higher temperature compared to test session only. This is because if the temperature of the session under temperature limit, that session has chances to increase the speed of testing by increasing test clock frequency through frequency scaling. Thus, the temperature becomes higher. Nevertheless, not all the session can be increasing the frequency because limited by the frequency of the slowest in the session and the temperature limit.

The maximum temperature was limited to 150°C. However, none of the session reaches that temperature limit. This is because only active cores under test dissipate power and the temperature values depends on the power values and heat transfer distribution on SoC. Advantages of DVFS technique are that it is possible to increase the test frequency as long as not exceed the structural frequency constraint and test power frequency constraint, besides temperature constraint. However, the limit of speed depends on the slowest core in that session or maximum over the session. If the frequency factor of a session is greater than 1, it shows that the session will produce less test time and higher temperature. If frequency factor, F_m is greater than 1, it indicates that the test frequency can still be raised to shorten test time. If F_m, smaller than 1, the maximum frequency on that session will be used. However, since the temperature of the session does not reach the limit, the frequencies all the sessions can be increased. Consequently, the test time was also reduced rapidly. This factor was influenced by the slowest frequency in the session. The important and critical part was test time, which is evaluated to show the effectiveness of the proposed method. It is presented in Column 4 to be compared with test time of session-based method in Column 8.

Table 1 - Comparison between DVFS and Frequency Scaling Technique

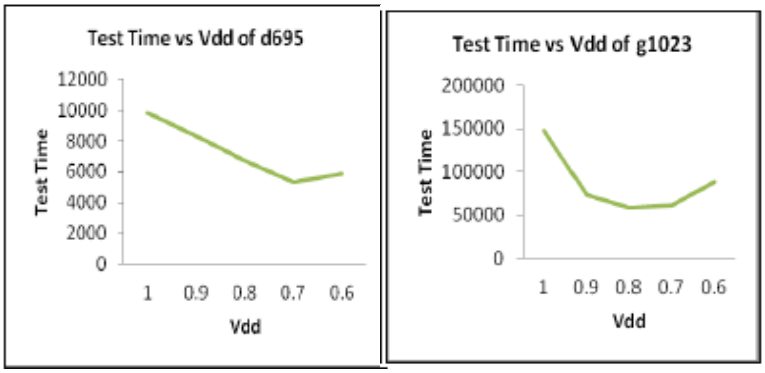
SoC Name	Test Session	Thermal Aware Test Scheduling Using DVFS		Test Session Technique [23]		Exploiting Technique [4]	
		Temp (°C)	Test Time (Arb)	Temp (°C)	Test Time (Arb)	Temp (°C)	Test Time (Arb)
d695	TS1=[C1,C2,C5, C6]	75	5306	75	9869	71	5874
	TS2=[C3,C4,C7,C10]	58	3034	57	5829	75	5874
	TS3=[C8,C9]	58	2476	54	4605	73	3470
g1023	TS1=[C1,C2,C3,C5]	138	2376	93	5939	64	274415
	TS2=[C4,C10,C11,C12]	92	5918	90	14794	65	3535
	TS3=[C6,C7,C8,C13]	92	710	88	1775	65	8806

	TS4=[C9,C14]	94	1794	88	4484	64	1057
h953	TS1=[C1,C2,C3,C4]	76	37299	114	119009	62	2669
	TS2=[C5,C6,C7,C8]	59	10637	59	34037	59	71046
a586710	TS1=[C1,C2,C3,C4,C5, C6]	76	4836963	53	7739141	38	20260
p34392	TS1=[C1]]	53	72458	68	170276	55	4606632
	TS2=[C2,C3,C4,C5,C6, C7,C8,C9]	60	125134	53	294064	73	101355
	TS3=[C10,C11,C12,C1 3,C14,C15,C16,C17]	62	231736	51	544579	71	324154
	TS4=[C18,C19]	59	5249	51	12336	51	7343

Table 2 - Optimum V_{dd} and Temperature Difference between Thermal Safe Test Scheduling using DVFS and Frequency Scaling only (using Nominal Voltage)

SoC Name	Nominal Voltage Set		Optimum Voltage Test		Test Time Reduction (%)
	Test Clock Freq	Test Time	Vdd Opt (V)	Test Time	
d695	1.01E-04	9.87E+03	0.7	5.31E+03	46
g1023	6.76E-06	1.48E+05	0.8	5.92E+04	60
h953	8.33E-06	1.19E+05	0.8	3.73E+04	61
a586710	1.29E-05	7.74E+06	0.7	3.79E+06	51
p34392	1.84E-06	5.45E+05	0.7	2.31E+05	58

Table 2 summarize the optimum V_{dd} and temperature difference between thermal safe test scheduling using DVFS and frequency scaling only (using nominal voltage). Based on the observations on the test time (in arbitrary unit), the result produced by DFVS is much faster compared to frequency scaling. This is because in DVFS, after reducing the voltage to optimum voltage, new power will be generated which is lower than original power. This is due to direct relationship between power and voltage, as in Equation (6). Furthermore, the result proved that the new test time after adjusting voltage will be much shorter compared to method that only scales the frequency without adjusting the voltage.



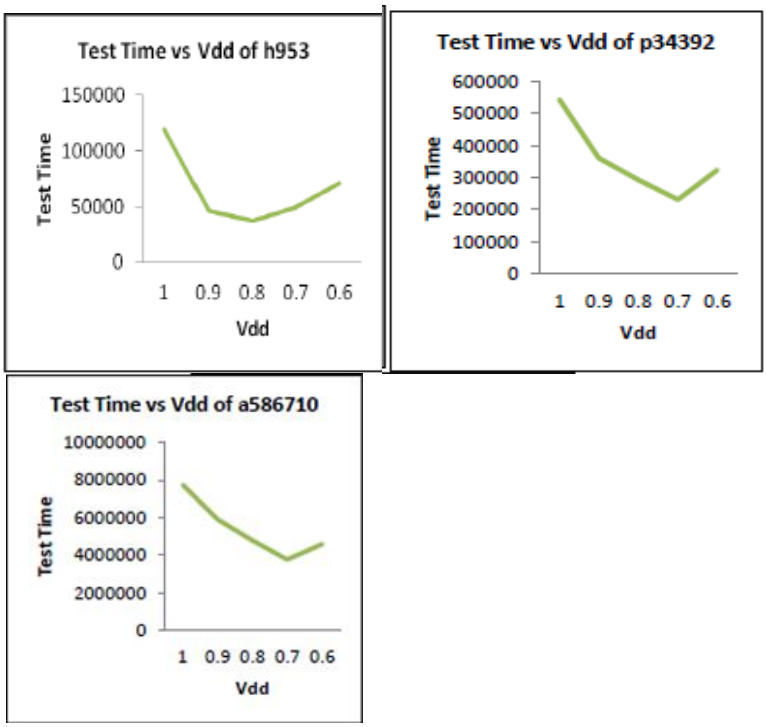


Fig. 4 - Test Time vs V_{dd} for five SoCs benchmark

The line graphs in Figure 4 shows the optimum test time versus V_{dd} for 5 SoCs benchmark. The first thing to note is that during lowest test time and optimal V_{dd}, the frequency constraint and power constraint is also on optimal value. Finally, test session and DVFS methods drives to a better test time result.

5. Conclusion

In this work, a method for the dynamic voltage and frequency scaling and the thermal aware task scheduling is considered. The results of optimization approaches to minimize the test time by applying DVFS technique with session-based test scheduling have been presented. This test scheduling is provided with thermal constraints to ensure temperature distribution in SoC is still under temperature limit. From the result, the proposed approach can lead to shorter test time and is capable of handling very tight thermal constraints compared to the thermal safe test scheduling presented by test session technique only. Results on different benchmark SoCs show have the effectiveness of our technique which produces shorter testing time. Total test time reduction by using proposed technique is 46% compared to frequency scaling technique altering the voltage supply.

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