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Performance Analysis of Nano Transistor Based Binary and Ternary Logic Gates

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Abstract

As technology scales down to the nanoscale regime, several short channel effects emerge, which have a greater impact on device performance. Researchers are exploring for innovative materials that can fit into nanometer-sized spaces to improve the performance of digital circuits. This paper provides Nano transistor-based digital circuits for improving digital circuit performance over traditional MOSFET-based circuits. Carbon nanotubes (CNTs) and graphene nano ribbons (GNR) have been investigated as possible candidates because to their high carrier mobility. The influence of CNTFET and GNRFET parametric variation with threshold voltage on performance metrics such as delay, and power has been investigated. A comparison of MOSFET, CNTFET, and GNRFET-based logic circuits is performed. A primer on ternary logic is also provided. Because of the dependence of the threshold voltage on the shape of carbon nanotubes and graphene nano ribbons, it is possible to use it for ternary logic design. Following that, ternary logic circuits are constructed with CNTFETs and GNRFETs. It has been determined that CNTFET and GNRFET-based circuits are more energy efficient than standard MOSFET circuits. It is also established that innovative ternary logic offers a relatively fast and low power digital circuit design option. All digital circuits were simulated using the HSPICE tool for the 32nm technology node.

1. Introduction

MOSFET is one of the most used semiconductor devices in VLSI design. However, at the nanometer regime, we can witness a lot of short channel effects that increase the leakage currents and power dissipation complications in small chips. Due to these many alternative nanometer technologies are being explored with a widespread intention to replace the existing MOSFET technology. CNTFET and GNRFET are the future technologies which are measured and have been planned for the replacement of the MOSFET technology. Many researchers are used in interconnect applications [1-3]. The CNTFET model includes the various parameters such as the allocation of carbon transmit speed and better mobility, then, it can be appropriate to various alternative circuits. It can also be used in integrated circuits, and it can cause low voltage, which results in lower power consumption and thereby improves its performance in comparison to MOSFET [4-7]. The CNTFET structure uses CNT as a channel in

between source and drain terminals like conventional MOSFET structure which is shown in Figure 1. Depending upon the number of CNTs may be used in the channel, it may be a SWCNT, or MWCNT depends upon the number of tubes that can be used as a channel [5].

The Semiconducting single walled CNTs can show a special interest because they are very capable in producing semiconducting devices that gadgets made by customary Si innovation. The CNTFET structure is relatively identical to silicon MOSFET aside from the CNT is associated with the transistor and acting as the channel. CNTFET works on the same principle as MOSFET, as the electrons travel from the source terminal to the drain terminal. This allows for the device to be operated in low powers as the device can be switched at smaller gate voltages [8-12]. The structure of GNRFET looks similar to the traditional MOSFET which is shown in Figure 2. The GNRFET consists of four terminals with gate, drain, source and bulk terminals. In which un-doped GNRs are placed under the gate terminal while heavily doped placed under source and drain terminals [13]. The device on and off conditions are based on the potential available at the gate terminal. The V-I characteristics of GNRFET are also the same as conventional MOSFET.

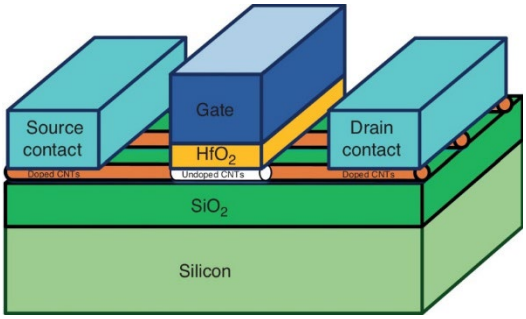

Fig. 1 *Structure of CNTFET*

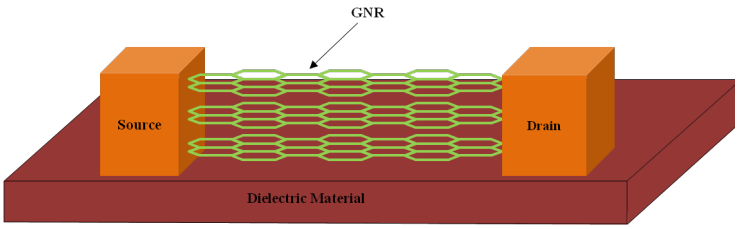

Fig. 2 *Structure of GNRFET*

The width (W) of GNR is calculated as:

$$W = (N + 1)\frac{\sqrt{3}}{2}a \quad (1)$$

Where, 'N' represents no of dimer lines which is proportional to width of GNR, 'a' is the lattice constant i.e., 0.142 nm. The dimer lines are inversely proportional to the band gap of GNR. The voltage that is required to turn ON the FET is called threshold voltage. The threshold voltage of GNRFET is inversely proportional to the width of GNR and is given as below.

$$V_{th} = \frac{E_g}{3e} \quad (2)$$

Where, $Eg = 2|\alpha|\Delta E$ is the band gap and e is the unit electron charge. α=0.27 for N=3P; α=0.4 for N=3P+1; α=0.066 for N=3P+2, $\Delta E = \frac{\hbar v_f \pi}{W}$, $\hbar = 6.5821 \times 10^{-16}$, v_f=10^6. For the dimer lines 6 the width of GNR is 0.86 nm and the threshold voltage is 0.43 V from (2). The width of GNR is calculated by dimer lines N using (1). The dimer lines of GNR increase as the width increases and the dimer lines is inversely proportional to band gap. GNRFETs provide equal opportunity to control threshold voltage by altering the width of GNR. We use multi width GNRFET design for ternary logic implementation. The Stanford GNRFET SPICE model is used for simulating the GNRFET based ternary logic gates. This is a SPICE model developed for unipolar, MOSFET-like GNRFET devices and it depends on the presumption of ballistic transport, which is just precise in a short channel GNRFET. In addition, it represents accurate and companionable GNRFET configurations for HSPICE simulations [14-16]. This paper presents the brief introduction to CNTFET and GNRFET in section 1. Binary logic gates are discussed in section 2. Ternary gates are discussed in Section 3. Finally, section 4 concluded this work.

2. Binary Logic Circuits and Device Characteristics

The current-voltage (I-V) characteristics of n-type CNTFET and GNRFET are simulated using HSPICE using CNT model is shown in Figure 3. From Figure 3 it can be depicted that the current-voltage (I-V) characteristic of CNTFET and GNRFET has a very similar trend like that of an nMOS. CNTFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The gate-source biasing modulates the non- tunneling potential barrier in the channel region, and thereby the good conductivity. Better gate electrostatics can be achieved by using high k, e.g. HfO2, gate dielectric material [17]. The CNTFET and GNRFET circuit performance changes with the diameter of CNT and number of GNR sheets, respectively. With

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varying chiral number (m, n) of the tube and number of GNR sheets (n), the drain current varies, which is shown in Figure 3. GNRFETs carry high current compared to CNTFETs because more GNR sheets can be placed in place of CNT tubes in FETs. Digital logic gates are important components in the construction of digital circuits. As a result, the focus of this study is on the design of logic gates employing binary logic and multi valued logic (MVL). First, several binary digital logic gates are simulated in HSPICE utilizing MOSFET, CNTFET, and GNRFET. Tables 1, 2, and 3 show the performance parameters of all logic gates, such as latency, average power, and peak power. It has been discovered that GNRFET-based logic gates have a lower delay than MOSFET and CNTFET-based logic gates. Hence the GNRFET based circuits are useful for designing of high-speed digital circuits as compared to other conventional gates. This is shown in Table 1.

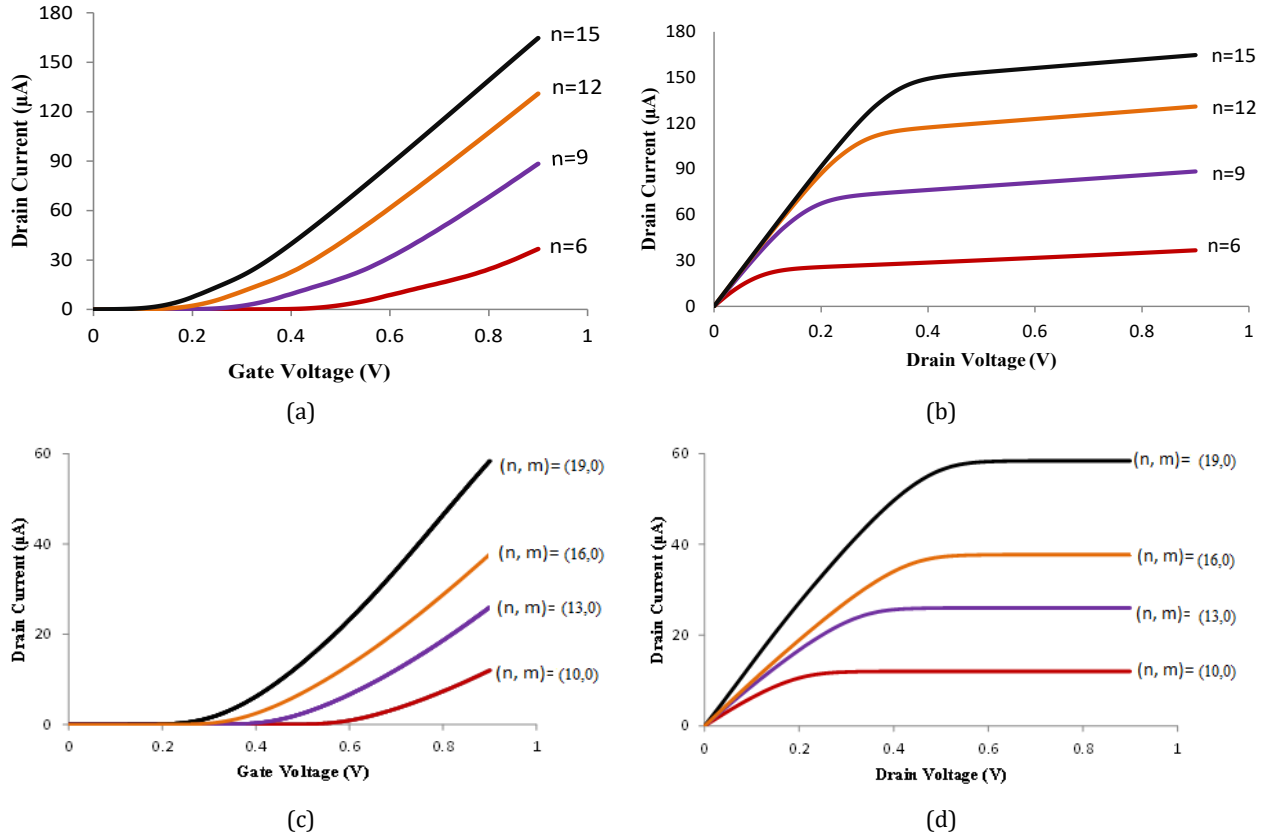


Fig. 3 *I-V characteristics of the GNRFET and CNTFET (a) Ids versus Vgs of GNRFET; (b) Ids versus Vds of GNRFET; (c) Ids versus Vgs of CNTFE; (d) Ids versus Vds of CNTFET*

Table 1 *Delay values of logic gates by using MOSFET, CNTFET, GNRFET (all values in seconds)*

Logic Gate	Type Of Transistor		
	MOSFET	CNTFET	GNRFET
Inverter	1.337E-11	1.946E-12	7.803E-13
NAND	3.511E-11	1.204E-11	8.826E-12
AND	1.013E-08	1.011E-08	1.010E-08
NOR	1.112E-11	1.282E-12	6.723E-13
OR	3.015E-08	3.011E-08	3.010E-08
XNOR	1.013E-08	2.730E-12	5.078E-13
XOR	2.004E-08	2.001E-08	4.940E-12

Table 2 *Average power values of logic gates by using MOSFET, CNTFET, GNRFET (all values in watts)*

Logic Gate	Type Of Transistor		
	MOSFET	CNTFET	GNRFET
Inverter	1.404E-07	3.470E-09	6.937E-08
NAND	1.782E-07	2.926E-09	1.101E-08
AND	3.976E-07	3.847E-09	1.056E-08
NOR	1.773E-07	2.217E-09	9.013E-09

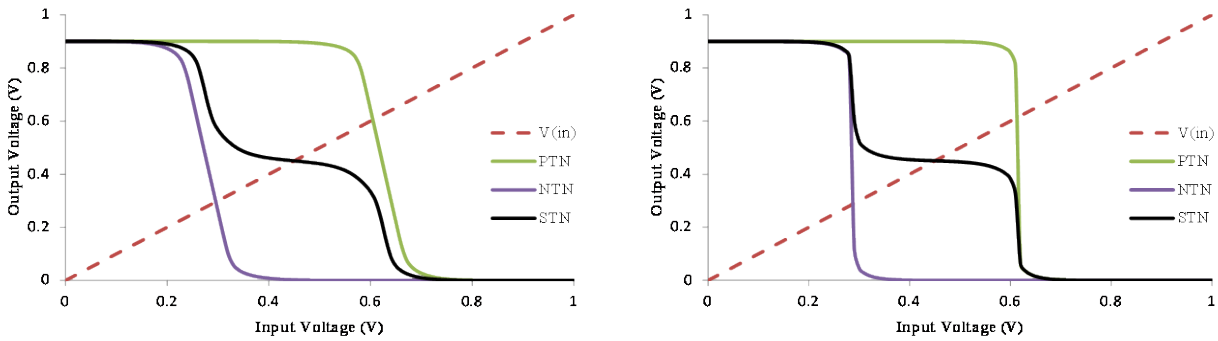
OR	3.618E-07	3.130E-09	1.511E-08
XNOR	7.976E-07	8.735E-09	3.635E-08
XOR	1.067E-06	1.133E-08	4.268E-08

3. Ternary Logic Circuits

Binary logic is a common approach for designing digital VLSI. However, circuit and system designers have been exploring multiple-valued logic (MVL) for several decades. More than two layers of logic can be accomplished using MVL circuits. The logic styles of MVL levels can be classed as ternary (base=3) or quaternary (base=4) [18-22]. In the current study, ternary logic has been established to create multi-threshold voltages in a circuit by varying the diameter of carbon nanotubes and the breadth of graphene sheets. Figure 4 depicts the voltage transfer characteristics (VTCs) for the three types of ternary inverters: STN, NTN, and PTN (standard, negative, and positive NOT gates) for both GNRFET and CNTFET. However, when it comes to power dispassion, CNTFET based circuits are showing a good result compared to conventional MOSFET and GNRFET as shown in Table 2 and Table 3. Depending on the application we can choose the technology like CNTFET and GNRFET. However, CNTFET has manufacturing difficulties as its tube type structure in comparison GNRFET. MOSFETs, GNRFETs, and CNTFETs are used to create ternary logic circuits in this study. Therefore, it was discovered that circuits developed and executed using GNRFETs gained less noise and delay than circuits built with MOSFETs and CNTFETs. Multi width GNRFETs are used in a GNRFET-based ternary logic system. Figure 5 depicts the STN, NTN, and PTN schematic diagrams. Logic 0, 1, and 2 correspond to voltage values of 0 V, 0.45 V, and 0.9 V, respectively. Figure 5 depicts the corresponding width and threshold voltages of each GNRFET. The STN outputs for both GNRFET and CNTFET are shown in Figure 6. For GNRFET and CNTFET based STN, the transistors widths, diameters and their corresponding threshold voltages are in Table 4. The threshold voltages with the variation of width and diameter are tabulated in Table 4 for both CNTFET and GNRFET.

Table 3 *Peak power values of logic gates by using MOS, CNTFET, GNRFET (all values in watts)*

Logic Gate	Type of transistor		
	MOSFET	CNTFET	GNRFET
Inverter	6.039E-05	2.792E-06	6.663E-06
NAND	1.066E-04	2.885E-06	7.178E-06
AND	2.229E-04	2.817E-06	1.256E-05
NOR	9.242E-05	3.087E-06	1.308E-05
OR	2.536E-04	5.404E-06	2.532E-05
XNOR	2.618E-04	7.472E-06	1.778E-05
XOR	2.954E-04	8.646E-06	2.454E-05



(a) (b)

Fig. 4 *VTC curves (a) GNRFET; (b) CNTFET*

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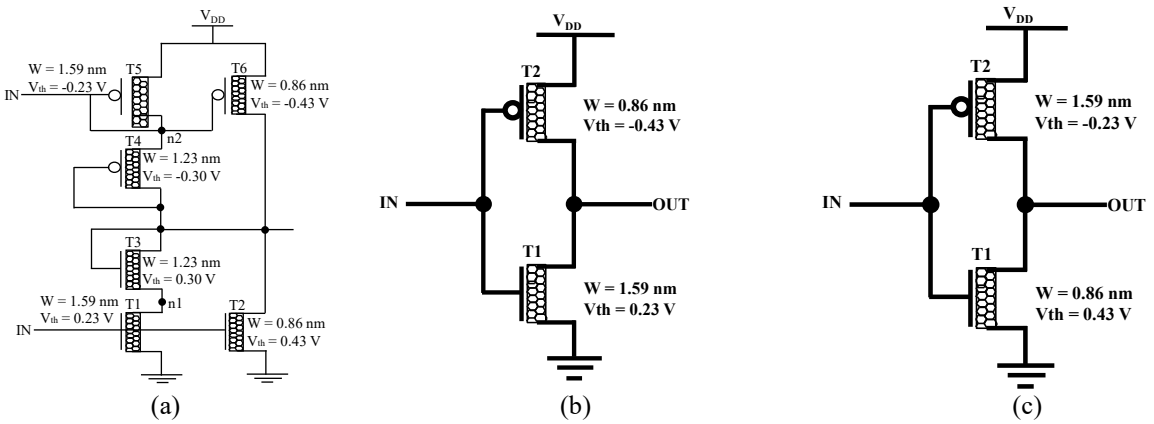


Fig. 5 GNRFET *based ternary inverters (a) STN; (b) NTN and; (c) PTN*

Delay is an essential consideration for both GNRFET and CNTFET-based digital circuits. The propagation delay is the lag time between input and output, and the delays from 0 to 1, 1 to 2, 2 to 1, 1 to 0, and their average from the input of GNRFET and CNTFET are presented in Table 5. Table 5 clearly shows that GNRFET-based circuits produce less latency than CNTFET-based circuits. The power consumption of GNRFET and CNTFET-based STNs, on the other hand, is 4.7450E-06W and 7.3231E-07W, respectively. The NTN outputs for both GNRFET and CNTFET are shownin Figure 7. For GNRFET and CNTFET based NTN, the transistors widths, diameters, and their corresponding threshold voltages are shown in Table 6.

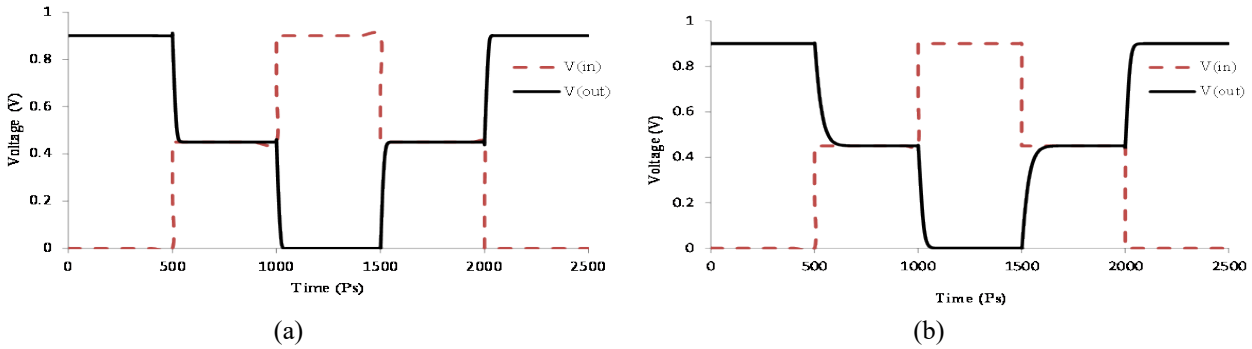


Fig. 6 *Output of STN (a) GNRFET; (b) CNTFET*

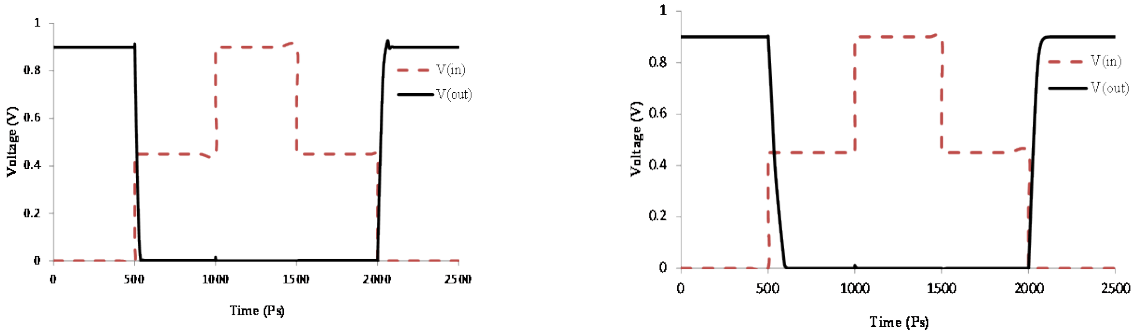
Table 4 *STN threshold voltages for both GNRFET and CNTFET*

Transistors	GNRFET		CNTFET	
	Width (nm)	Threshold Voltage (V)	Diameter (nm)	Threshold Voltage (V)
T1	1.59	0.23	1.48	0.28
T2	0.86	0.43	0.78	0.55
T3	1.23	0.30	1.01	0.42
T4	1.23	-0.30	1.01	-0.42
T5	1.59	-0.23	1.48	-0.28
T6	0.86	-0.43	0.78	-0.55

Table 5 *Propagation delay of STN*

Input Switching Activity	Delay	
	GNRFET (ps)	CNTFET (ps)
0-1	10.371	59.446
1-2	10.758	38.934

2-1	10.477	56.377
1-0	10.612	34.205
Average	10.554	47.240



(a) (b)

Fig. 7 *Output of NTN (a) GNRFET; (b) CNTFET*

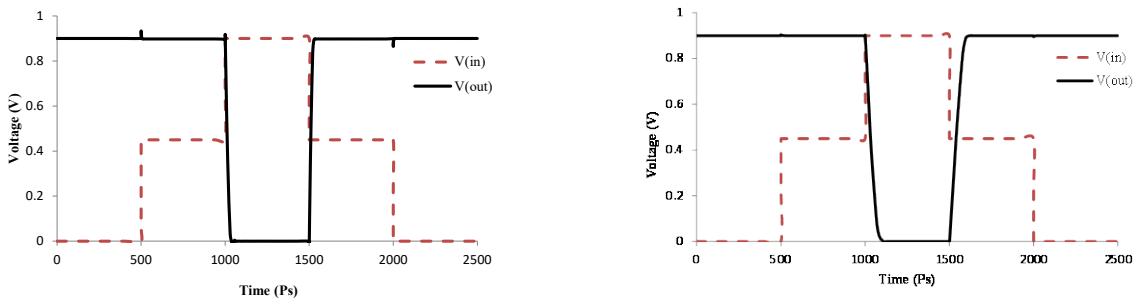
Table 7 shows the delays from 0 to 1 and 1 to 0, as well as their average delay from the input of GNRFET and CNTFET. Table 7 clearly shows that GNRFET-based NTN circuits produce less delay than CNTFET-based NTN circuits. The power consumption of GNRFET and CNTFET-based NTNs, on the other hand, is 1.1311E-06W and 2.9011E-07W, respectively. Figure 8 depicts the PTN outputs of both the GNRFET and the CNTFET. Table 8 shows the transistor widths, diameters, and threshold voltages for GNRFET and CNTFET-based PTN. Table 9 shows the delays from 1 to 2 and 2 to 1 as well as their average delay from the input of GNRFET and CNTFET. Table 9 clearly shows that GNRFET-based PTN circuits produce less latency than CNTFET-based PTN circuits. The power consumption of GNRFET and CNTFET-based PTNs, on the other hand, is 1.2604E-06W and 2.8503E-07W, respectively.

Table 6 *NTN threshold voltages for both GNRFET and CNTFET*

Transistors	GNRFET		CNTFET	
	Width (nm)	Threshold Voltage (V)	Diameter (nm)	Threshold Voltage (V)
T1	1.59	0.23	1.48	0.28
T2	0.86	-0.43	0.78	-0.55

Table 7 *Propagation delay of NTN*

Input Switching Activity	Propagation Delay NTN	
	GNRFET (ps)	CNTFET (ps)
0 – 1	7.4210	47.109
1 – 0	9.8864	33.605
Tp	8.6537	40.357



(a) (b)

Fig. 8 *Output of PTN (a) GNRFET (b) CNTFET*

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Table 8 *PTN threshold voltages for both GNRFET and CNTFET*

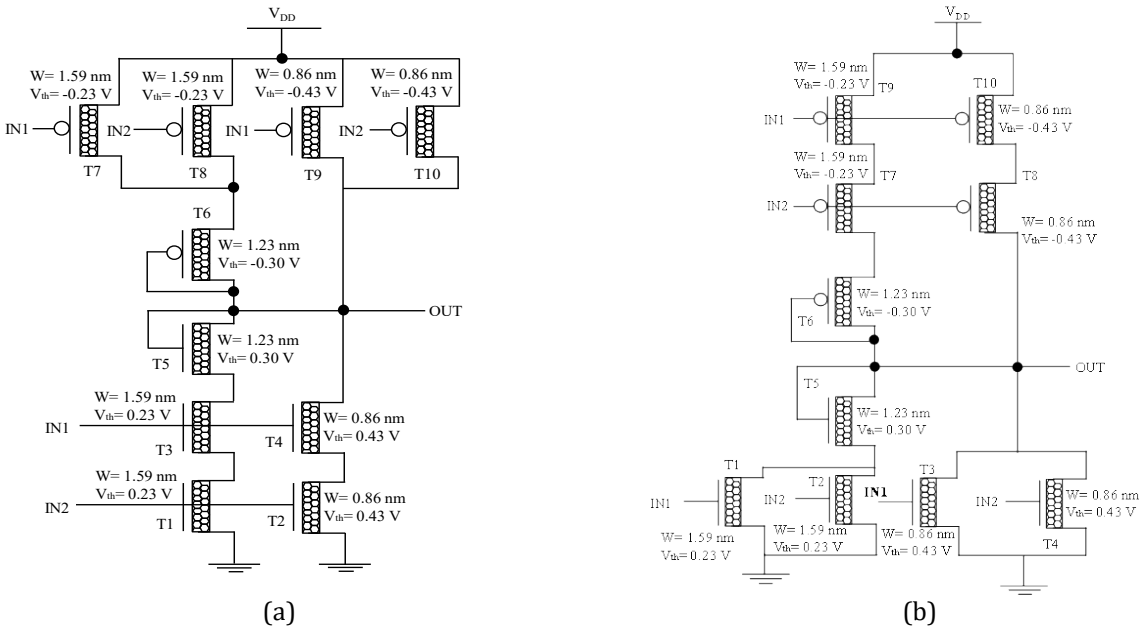
Transistors	GNRFET		CNTFET	
	Width (nm)	Threshold Voltage (V)	Diameter (nm)	Threshold Voltage (V)
T1	0.86	0.43	0.78	0.55
T2	1.59	-0.23	1.48	-0.28

Table 9 *Propagation delay of PTN*

Input Switching Activity	Propagation Delay PTN	
	GNRFET (ps)	CNTFET (ps)
1 – 2	10.001	37.968
2 – 1	7.4976	46.097
Tp	8.7495	42.033

4. Ternary NAND and NOR Gates

The arithmetic circuits are designed with the help of basic gates like AND, NAND, NOR, OR and NOT. The focus of this work is on the NAND and NOR because they are universal gates. The two input GNRFET NAND and NOR gates are shown in Figure 9. The circuit diagram of NAND and NOR gates consist of ten GNRFET's with three different widths of 1.59 nm, 1.23 nm, 0.86 nm have threshold voltage of 0.23 V, 0.30 V, 0.43 V. The operation of NAND is when any one of the inputs is less than the 0.23 V then the output is high, when the inputs are in between 0.23 V and 0.42 V the output is middle but not for when both inputs are high. If both inputs are high, then the output is low. The operation of NOR is when any one of the inputs is greater than 0.42 V then the output is low, when the inputs are in between 0 V to 0.23 V the output is middle but not when both inputs are 0 V and when both inputs are 0 V the output is high. We considered the delays from 1 to 2, 0 to 1 for the first-time rise, 0 to 1 for the second time rise and 1 to 2 and their average delay from the input of GNRFET and CNTFET shown in Table 10. By observing the TABLE 10, GNRFET based NAND circuit provides less delay compared to CNTFET NAND based circuits. However, Power Consumption of CNTEFT and GNRFET based NAND gates is 3.9445E-06W and 5.0800E-07W. The simulation output waveforms of ternary Nand gate using GNRFET and CNFET are shown in figure 10. We considered the delays from 0 to 1, 0 to 1, 1 to 2 and 1 to 2 and their average delay from the input of GNRFET and CNTFET shown in Table 11. By observing Table 11, GNRFET based NOR circuit provides lesser delay compared to CNTFET based NOR circuits. However, the Power Consumption of CNTFET and GNRFET based NOR gate is 3.8736E-06W and 5.0555E-07W. The simulation output waveforms of ternary NOR gate using GNRFET and CNFET are shown in figure 11.



(a) (b)

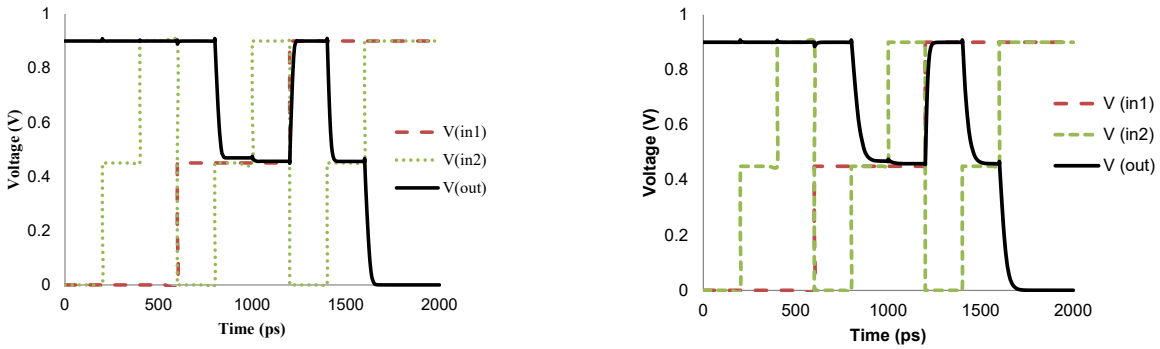
Fig.9 *GNRFET based NAND and NOR gates (a) Schematic diagram of NAND; (b) Schematic diagram of NOR*

Table 10 Propagation *delay of ternary NAND gate*

Input Switching Activity	Propagation Delay Ternary Nand gate	
	GNRFET (ps)	CNTFET (ps)
1 – 2	3.9522	8.5830
0 – 1	606.03	630.20
0 – 1	604.35	622.21
1 – 2	1205.8	1223.8
Tp	605.03	621.21

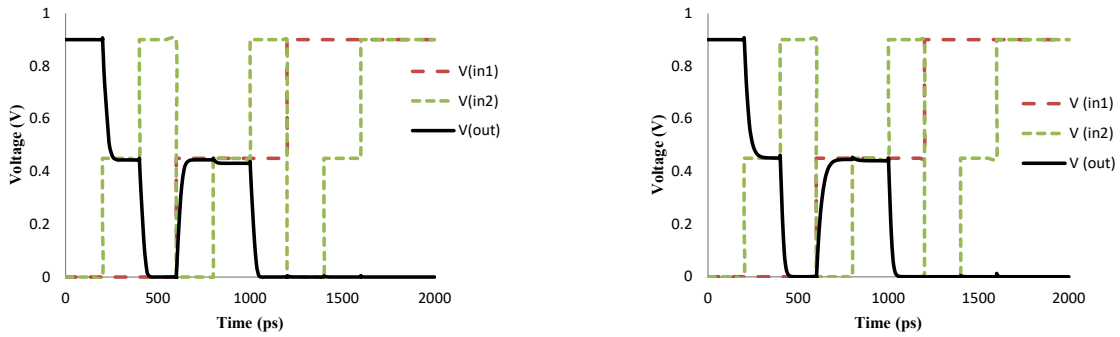
Table 11 *Propagation delay of ternary NOR gate*

Input Switching Activity	Propagation Delay Ternary Nor gate	
	GNRFET (ps)	CNTFET (ps)
0 – 1	3.4789	18.402
0 – 1	3.7752	18.235
1 – 2	3.6894	12.732
1 – 2	3.5297	12.176
Tp	3.6183	15.386



(a) (b)

Fig. 10 *Simulated results of NAND gate (a) GNRFET; (b) CNTFET*



(a) (b)

Fig. 11 *Simulated results of NOR gate (a) GNRFET; (b) CNTFET*

5. Conclusion

This work presented a Nano transistor based digital circuits to improve the performance of the digital circuits as compared to the conventional MOSFET based circuits. Carbon nanotubes (CNTs) and graphene nano ribbon (GNR) have been explored as a promising candidate for the same due to their excellent carrier mobility. The effect of CNTFET and GNRFET parametric variation with threshold voltage on performance metrics namely delay and power has been analyzed. A comparative study of MOSFET, CNTFET and GNRFET based logic circuits is carried out.In GNRFETs the threshold voltage can be organized by the width commonly defined by the number of dimer lines, whereas in CNTFET it can be controlled by diameter which depends on the chirality vector. The standard, positive and negative NOT gates along with the universal gates are designed using industry standard HSPICE to achieve propagation delay and power. The circuits designed and implemented using GNRFETs consume lesser delay over the circuits designed by the CNTFET since the GNRFET offers high currents.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

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