INTERNATIONAL JOURNAL OF INTEGRATED ENGINEERING
ISSN: 2229-838X e-ISSN: 2600-7916

IJIE

Vol. 17 No. 2 (2025) 177-185
https://publisher.uthm.edu.my/ojs/index.php/ijie

Characterization and Optimization of Si-FinFET Structure Based on Gate Length and Working Temperature

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DOI: https://doi.org/10.30880/ijie.2025.17.02.014

Article Info

Received: 14 August 2024
Accepted: 13 July 2025
Available online: 28 July 2025

Keywords

Si-FinFET, temperature, sensitivity, MuGFET, nano-sensor

Abstract

This research explores the potential of utilizing Fin Field Effect Transistors (FinFETs) as nano-scale temperature sensors, with a focus on their temperature sensitivity. The thermal characteristics of FinFETs were rigorously analyzed using the Multi-gate Field Effect Transistor (MuGFET) simulation engine. Temperature sensitivity was evaluated by examining the mode coupling of the metal-oxide-semiconductor (MOS) diode during simulations of current-voltage (I-V) behavior across varying gate lengths (Lg = 7, 10, and 20 nm) and temperature ranges. The maximum temperature sensitivity of the FinFET is determined by identifying the largest ΔI within the operating voltage range of 0-1 V (V_{DD}). Notably, the temperature sensitivity of FinFETs increases proportionally with channel length, within the 7 to 20 nm range. Based on the results, the optimal channel length for maximizing temperature sensitivity under the specified conditions is 10 nm. These findings offer valuable insights into the design parameters of FinFETs for enhanced thermal responsiveness.

1. Introduction

As metal oxide semiconductor field-effect transistors (MOSFETs) approach the fundamental limits of their downscaling, significant research efforts have shifted towards exploring a diverse array of advanced FET (field-effect transistor) architectures. Among these, the FinFET, a fin-structured FET, stands as a prominent recent innovation, yet it poses several challenges in optimization—both in theoretical modeling and within the semiconductor fabrication domain [1-5]. FinFET technology has generated considerable interest from industry stakeholders due to its versatile applications, spanning sensors and switching devices. A prime example of an embedded sensor leveraging semiconductor technology is the temperature sensor [6], often integrated within equipment. Temperature sensors based on nanowire transistors are designed by analyzing the current-voltage characteristics of these transistors under varying thermal conditions [7-10]. By shorting the base and collector terminals of a bipolar transistor and operating it as a diode, precise temperature measurements can be achieved. Similarly, in MOSFET-based sensors, the transistor's gate can be connected to either the source or drain terminal to function as a temperature-sensitive component. The proliferation of diodes, resistors, capacitors, and transistors in modern electronics is driven by their ability to form ultra-compact circuits.

The efficiency of these cutting-edge technologies is often contingent upon their nanoscale properties, which enable a broad spectrum of novel applications. As future research yields further insights, these exceptionally potent electronic devices—featuring astonishingly small transistors integrated onto chips—are likely to become increasingly reliable and indispensable. While the traditional MOSFET paradigm is nearing its practical

boundaries, it remains a revolutionary technology. However, continued exploration into nanoscale FET architectures is imperative, with further advancements in research, development, and fabrication techniques being critical to unlocking their full potential. In circuit design, FinFETs present distinct advantages over conventional bulk silicon devices [11]. Complete depletion of SOI (Silicon-On-Insulator) has been observed at elevated temperatures of 275–300°C, although partially depleted SOI can endure up to 225°C, while bulk silicon withstands up to 200°C. Certain integrated circuits (ICs), such as those embedded in oil drill bit sensors or automotive systems near engine blocks, are required to function reliably under high thermal loads.

Recent research has predominantly focused on thermal conductivity and its implications on the electrical performance of FinFETs [12]. In particular, further investigation into FinFET devices has emphasized the effects of body, drain, and gate biases on thermal behavior and power dissipation [12]. While conventional planar transistors suffer from inherent limitations, the advent of FinFET technology has been instrumental in mitigating short-channel effects and enabling the production of highly miniaturized semiconductor devices, down to nanoscale dimensions. One critical challenge that hinders the efficiency of FinFETs is self-heating, an issue exacerbated by the 3D geometry of the device. This thermal effect degrades the overall performance of the semiconductor, making it imperative for manufacturers to rigorously assess heat's impact on device reliability and operational efficacy. Due to the vast number of transistors in modern integrated circuits, numerical simulation of FinFETs poses a considerable challenge. Effective electrothermal modeling requires generating detailed temperature profiles across the device, which can only be achieved by dividing the structure into uniform segments and ensuring continuity of temperature and heat flux across interfaces.

Treating heat dissipation as a loss across the FinFET width creates avoidable inefficiencies due to the homogeneity in power generation. Once the thermal solution for each segment is derived, a thermal circuit for the FinFETs can be established. This approach yields temperature profiles in the absence of gate control. Preliminary analyses from finite element simulations reveal minor discrepancies in thermal behavior, suggesting that these models have significant potential for precision. Despite being in their early stages, these results show promise in developing robust models for accurate temperature prediction [13]. Furthermore, the gate dielectrics are co-fabricated, significantly reducing contamination risks. Gate misalignment is minimized since lithographic exposure and patterning for the gate electrodes occur in a unified process. The top-down nature of FinFET integration inherently leads to the use of traditional materials, rather than conventional CMOS, for device fabrication. However, FinFET fabrication is constrained by the etching process, which governs the device's width and thickness. This results in slight deviations when compared to standard SOI devices.

As the complexity of device architectures increases, a deeper understanding of the underlying physics demands more sophisticated electronic device simulations. This study employs simulation methodologies to evaluate the performance and investigate the limitations of nanowire architectures. Simulation tools complement experimental efforts, particularly in characterizing MuGFETs at nano-scale dimensions [14]. Moreover, these simulations provide insight into the advantages and drawbacks of various device configurations, facilitate cost-reduction strategies, and demonstrate the scalability of devices operating at the nanometer scale [15, 16]. The FinFET is frequently described in terms of a multi-gate transistor design, regardless of whether gates are present or not. Table 1 summarizes the advantages of FinFET. This paper discusses the selection of channel dimensions as well as the effects of oxide thickness, width, and length on electrical properties.

Table 1 *Advantages of FinFET*

Parameters	Details
Power	Greater degrees of integration are made possible by reduced power consumption. Early adopters claimed a 150% improvement.
Operating voltage	The low VT of FinFETs causes them to run at a low voltage.
Feature size	permits crossing the 20 nm barrier, which was previously believed to be the end point.
Static leakage current	Reduced by up to 90% on average
Operating speed	FinFET variants are typically 30% quicker than non-FinFET counterparts.

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2. Research Method

The finFET structure that was investigated in this research is shown in Figure 1. The features of the FinFET transistor were examined in this study using MuGFET as a modeling tool. Under various circumstances and with various settings, the output characteristic curves of the transistor were analyzed. The simulation-derived I-V physical characteristics were used to study the effects of different parameters on the nanowire transistor, such as temperature and gate length. For FETs with nano-dimensional architectures, Purdue University's MuGFET [17] simulation program was employed.

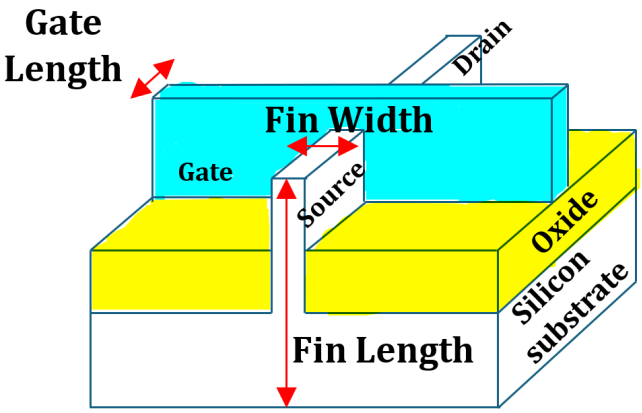

Fig. 1 *FinFET structure*

Bell Laboratories developed PADRE and PROPHET, two advanced simulation tools integrated within MuGFET's capabilities. PADRE is a versatile device simulator designed for two- or three-dimensional devices with adaptable geometries, while PROPHET is an equation-based solver applicable to one, two, or three dimensions [17]. These software tools offer researchers valuable insights by generating representative FET output curves, especially when the physics of FET operation is accurately modeled. Leveraging MuGFET, transport dynamics can be simulated based on independent responses to drift-diffusion models [18]. The MuGFET nanoHUB was created and approved by Purdue University, one of the top research universities in this area. MuGFET tool is reliant on simulating Nanoscale Multigate-FET architectures (Nanowire and FinFET) utilizing drift-diffusion methods. Due to the high cost of nanodevices and the extensive body of research relying on simulation utilizing MuGFET, researchers used this technology to prevent losses in nanodevices [19-20].

To replicate the Id-Vg properties of FinFETs at various temperatures, the MuGFET simulation was employed the subsequent attributes: channel concentration (P-type), Channel width, drain length and source, drain concentration (N-type) and source. Oxide thickness and gate length. An illustration of the FinFET environment could be found in Figure 2 [21-22].

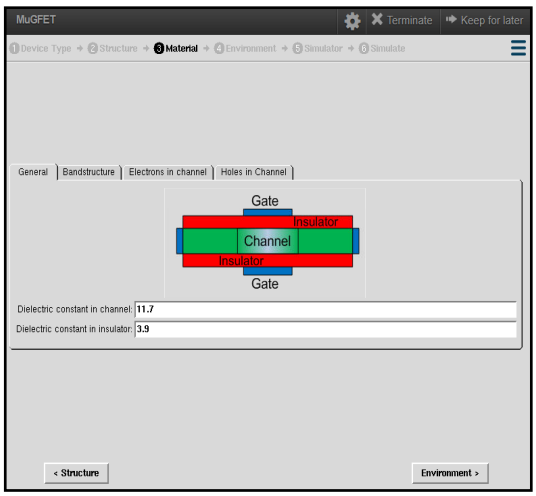

Fig. 2 *Homepage of MuGFET simulation tool*

The following parameters were employed to simulate the Id-Vg characteristics of FinFETs at temperatures of 275, 300, 325, and 350 K: a 1 nm oxide layer, drain and source lengths of 5 nm, and uniformly N-type concentrations. The channel diameter was set to 3 nm, with a gate doping concentration of 10^{19} cm^{-3}. Within the operating voltage range of 0–1 V, the maximum current variation (ΔI) is utilized to identify the FinFET's optimal temperature sensitivity. Additionally, increased oxide thickness results in a reduced drain-induced barrier lowering (DIBL) and a corresponding shift in the threshold voltage. The electrical behavior, relative to width variation, is illustrated in Figure 3.

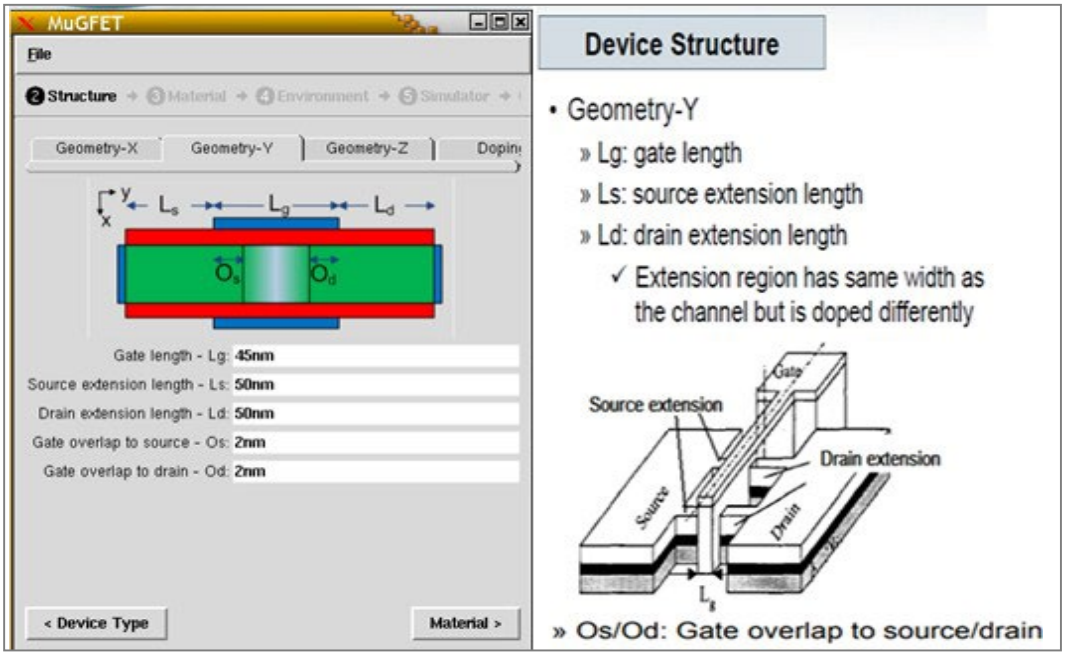

Fig. 3 *Selection of channel length*

3. Results and Discussion

Figures 4(a through c) depict the variation in current (I) as a function of gate lengths (Lg) of 7, 10, and 20 nm, with voltage increments of 0.1 V. As temperature increases within the VDD range of 0 to 1 V, the figures reveal a linear decrease in V_{DD} with rising temperature, with maximum sensitivity (max ΔI) observed at lower temperatures. Figures 4 (a) and (b) illustrate the optimal temperature sensitivity coefficients at V_{DD} = 0.6 V for Lg values of 7 nm and 10 nm, respectively, while Figure 4 (c) demonstrates the lowest sensitivity at Lg = 20 nm for VDD = 0.6 V. These results underscore that the most favorable operating condition for the transistor, with stability across the 325–350 K temperature range, occurs at a drain voltage (Vd) of 0.6 V, as indicated in Figures 4 (a) to (c). Figures 4 (d) through Figures 5(b) present the variations in ΔI with decreasing V_{DD} at T = 275, 300, 325, and 350 K for gate lengths of 7, 10, and 20 nm. The highest sensitivity (max ΔI) is observed at V_{DD} values of 0.4 V (Lg = 7 nm), 0.5 V (Lg = 10 nm), and 0.53 V (Lg = 20 nm). These figures conclusively show that ΔI increases with both rising temperature and V_{DD}, with the optimal voltage observed at 0.4 V for Lg = 10 nm and Wg = 3 nm.

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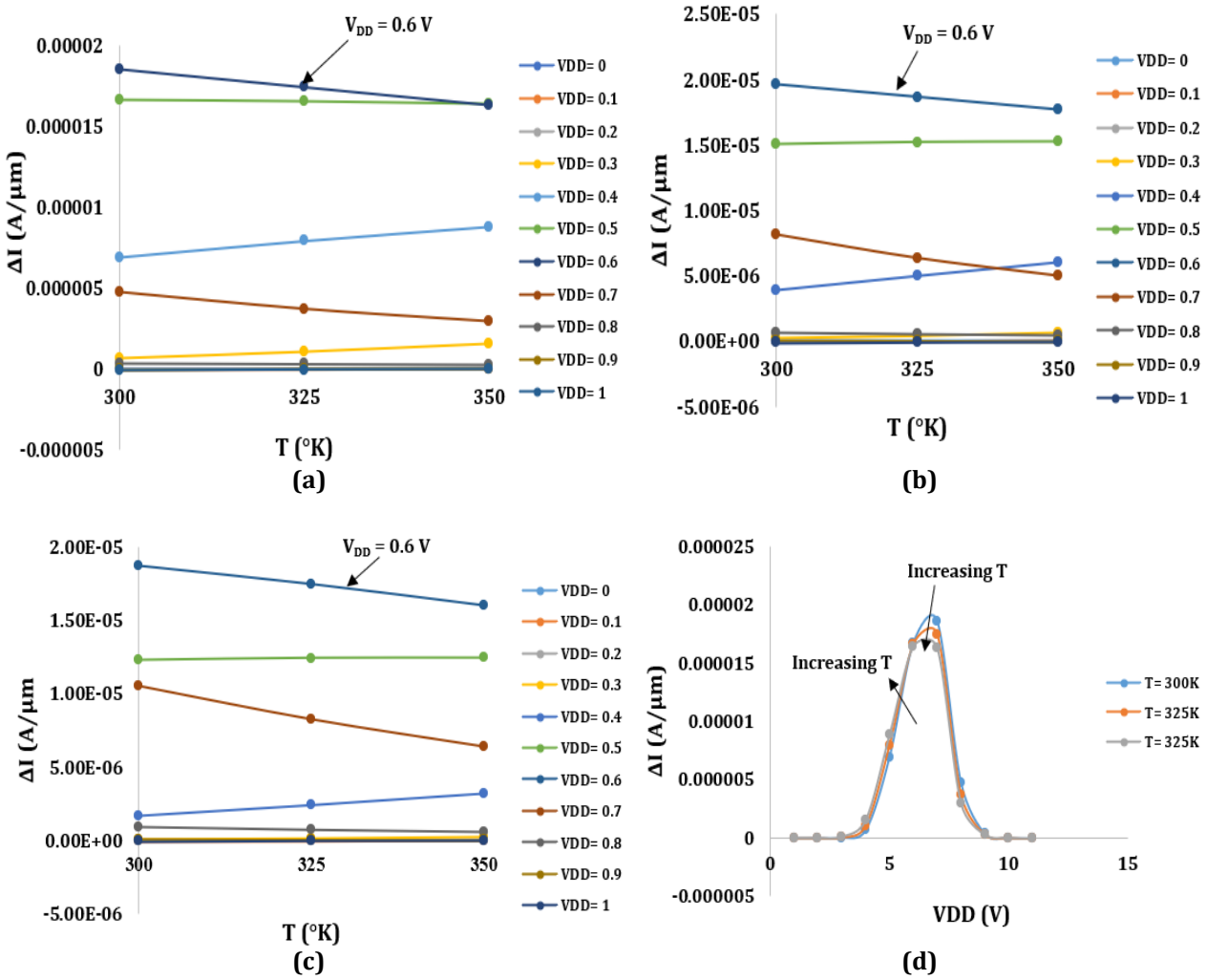

Fig. 4 *(a) ΔI–T characteristics of FinFET (Wg=3nm, Lg = 7nm); (b) ΔI–T FinFET characteristics (Wg =3nm, Lg=10nm); (c) ΔI–T FinFET characteristics (Wg =3nm, Lg=20nm); (d) ΔI–V_{DD} characteristics of FinFET (Wg =3nm/ Lg = 7nm)*

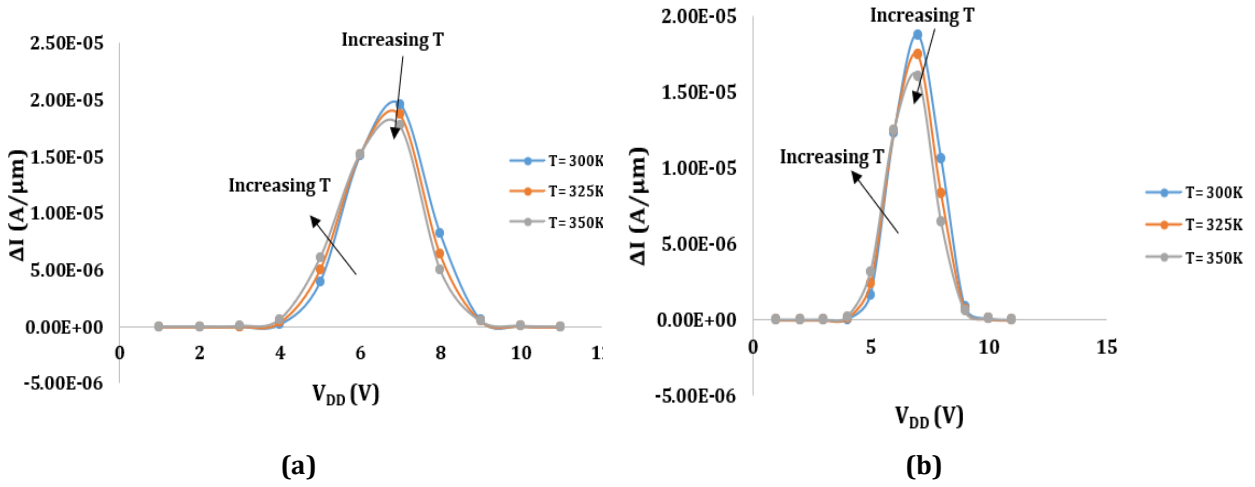

Fig. 5 *(a) FinFET characteristics (Wg=3nm, Lg = 10nm) ΔI–V_{DD}); (b) FinFET characteristics (Wg = 3 nm, Lg = 20 nm) ΔI–V_{DD})*

Figure 6(a) illustrates the ideal operating voltage (V_{DD}) corresponding to the highest thermal sensitivity observed in Figures 8–10, as a function of channel length and optimal temperature sensitivity. Although the channel length increased slightly from 7 nm to 20 nm, the temperature sensitivity showed a pronounced increase up to Lg = 10 nm. Beyond this point, the relationship between channel length and temperature sensitivity displayed a linear decline. Figure 6(b) presents the temperature profiles for key parameters, including subthreshold swing (SS), threshold voltage (V_T), and drain-induced barrier lowering (DIBL) of the FinFET, measured at temperatures of 275, 300, 325, and 350 K with Lg = 7 nm. As temperature increased, V_T demonstrated a linear decline, with values dropping from 0.47 V at 275 K to 0.43 V at 350 K. This decline in V_T, due to the reduction in the potential barrier within the channel at the source, results in an increased drain voltage (V_{DD}) and higher leakage current in the OFF state, as DIBL diminishes V_T. At the lowest temperature of 275 K, SS was measured at 91.08 mV/dec, rising to 117.90 mV/dec at 350 K, which is the furthest deviation from the ideal SS of 69.5 mV/dec. Conversely, 350 K approaches the optimal SS value of 54.6 mV/dec. Additionally, DIBL exhibited an exponential increase with rising temperature. Consequently, this study identifies the optimal transistor dimensions at Lg = 7 nm and 20 nm. With increasing oxide thickness, SS increased linearly, DIBL surged exponentially, and V_T followed a hyperbolic growth pattern.

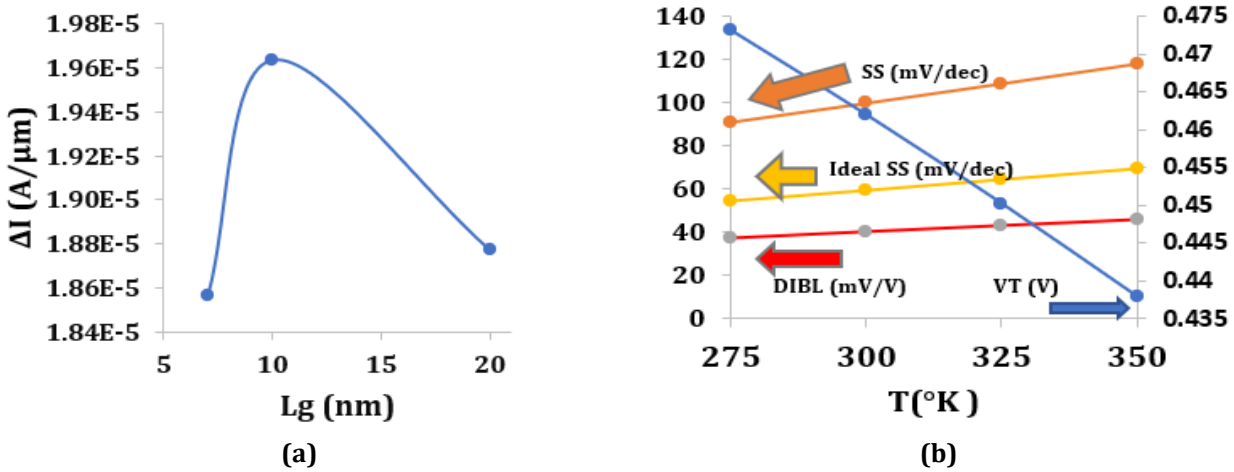

Fig. 6 *(a) Based on the highest temperature sensitivity, the operating voltage V_{DD} was optimized using a range of channel lengths); (b)* V_T, DIBL and SS at Wg =3nm, Lg = 7 nm*)*

Figure 7 (a) illustrates the FinFET's V_T, SS, and DIBL behaviours at temperatures of 275, 300, 325, and 350 K, and a gate length (Lg) of 10 nm. The graph reveals a linear decrease in these parameters as the temperature rises from 275 to 350 K. Specifically, SS ranges from 77.77 to 104.06 mV/dec, DIBL from 12.78 to 17.35 mV/V, and V_T from 0.50 to 0.47 V. At 325 K, SS reaches 77.77 mV/dec, which represents the most significant deviation from the optimal SS value of 54.6 mV/dec. SS is shown to be temperature-dependent, increasing to 85.34 mV/dec as the temperature rises, reflecting its distance from the ideal SS. Similarly, DIBL exhibits an upward trend in correlation with temperature. Figure 7(b) further demonstrates the relationship between V_T, DIBL, and SS variations, and their cumulative effects on the FinFET's performance at temperatures ranging from 275 to 350 K, with Lg = 20 nm. As the temperature increases, V_T decreases linearly, with values ranging from 0.53 V at 275 K to 0.49 V at 350 K. SS increases from 69.57 to 89.27 mV/dec, and DIBL rises from 2.56 to 3.71 mV/V. At 325 K, the SS value of 69.57 mV/dec is closest to the optimal SS of 54.6 mV/dec. However, at 350 K, SS increases further to 89.27 mV/dec, and DIBL continues to rise with temperature, reflecting their impact on the device's electrical characteristics. The electrical properties are used to determine the combination of optimal length and temperature.

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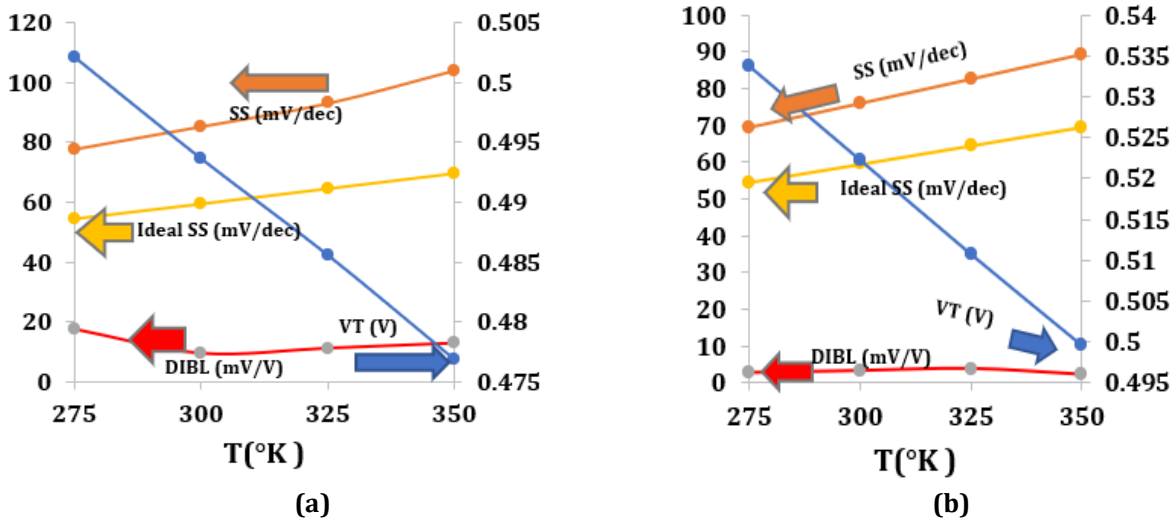

Fig. 7 *(a)* V_T, SS and DIBL at Wg=3nm, Lg = 10 nm.*); (b)* V_T, SS and DIBL at Wg =3nm, Lg = 20 nm.*)*

Figure 8 provides insights into the behavior of V_T, DIBL, and SS at different FinFET channel lengths, varying from 7 to 20 nm at 300 K. V_T increases until it reaches saturation beyond a channel length of 10 nm, while DIBL significantly decreases near 10 nm before slightly rising afterward. SS decreases and approaches the ideal value at 10 nm, suggesting that this is the optimal channel length for FinFETs under the tested conditions. The figure indicates that as temperature rises, SS increases while V_T and DIBL decrease, reaffirming that a channel length of 7 to 10 nm is ideal. These results corroborate previous studies [23]. showing that FinFET channel dimensions between 7 and 20 nm are linearly proportional to their electrical properties.

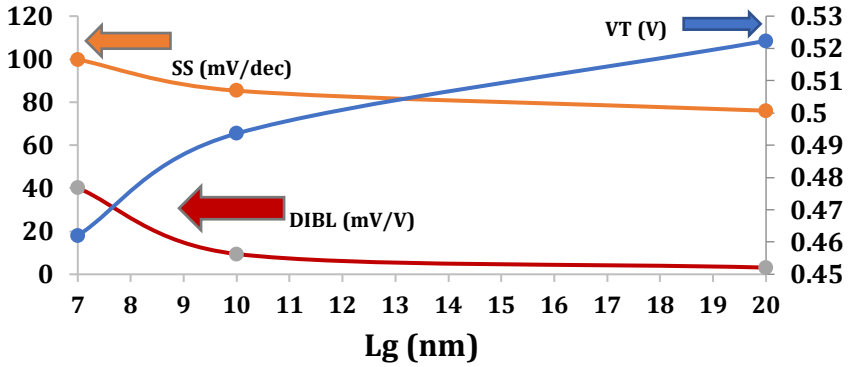

Fig. 8 *V_T, SS and DIBL with Lg*

Temperature is identified as the most significant factor influencing the current in FinFETs, primarily due to the higher carrier velocity observed in n-type FinFETs as fin diameters decrease. Notably, scaling the channel cross-section has a negligible effect on carrier velocities in n-type FinFETs. In aggressively downscaled MOSFETs, the effective carrier injection velocity (Vinj) governs the drain saturation current from source to channel. This carrier injection velocity, a material property distinct from mobility, plays a crucial role in determining the drive current during ballistic transport [24]. Table 2 shows a comparison of FinFET results with those from other studies.

Table 2 *Comparison with other research works*

Reference	Best value of SS	Best value of DIBL
[24]	72.43 mv/dec	139.52 mv/V
[25]	80 mv/dec	10 mv/V
[26]	73 mv/dec	28mv/V
[26]	60 mv/dec	10 mv/V
Present study	85.3 mv/dec	9.4 mv/V

4. Conclusion

By evaluating various channel lengths (Lg = 7, 10, and 20 nm), the influence of different temperatures (275, 300, 325, and 350 K) on FinFET performance is systematically analyzed. The diode-mode transistor configuration demonstrates that increasing the channel length up to 20 nm results in the most pronounced temperature-dependent current variations (ΔI). Beyond this point, the current values remain constant irrespective of channel length. At temperatures of 275, 300, 325, and 350 K, the characteristics of V_T, DIBL, and SS were studied across FinFET channel lengths ranging from 7 to 20 nm. As the channel length exceeded 10 nm, V_T exhibited an increase, approaching saturation; SS diminished, nearly achieving its optimal value; and DIBL reduced significantly as it near to 10 nm, before marginally rising above this length. According to the investigation's results, 10 nm is the ideal channel length for FinFETs with superior V_T, DIBL, and SS in the examined circumstances. This study paves the way for future research into gate operation adjustments and mesh spacing parameters to further enhance the performance of FinFETs with shorter gate lengths.

Acknowledgement

The author would like to thank Universiti Teknologi MARA, Malaysia, and A'Sharqiyah University, Oman, for cooperating in this research.

Conflict of Interest

The authors state that there is no conflict of interest with the publishing of the work.

Author Contribution Statement

Investigation, Writing - Original Draft, Resource, Formal analysis: *Yousif Atalla;* ***Review & Editing, Conceptualization, Supervision:*** *Mohamad Hafiz Mamat;* ***Validation, Resource, Co Supervision, Methodology, Conceptualization:*** *Yasir Hashim*

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