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Design of a High Efficiency Single-Bit Full Adder Using Modified Gate Diffusion Input (MGDI) Technique

Wai-Leong Pang[1], Seyed Arash Zareianjahromi[2], Swee King Phang[1], Ajay Kumar Singh[3], Angie See Tien Ng[4], Kah-Yoong Chan[2]*

[1] *School of Engineering, Taylor's University, Subang Jaya, 47500, MALAYSIA*
[2] *Centre of Advanced Devices and Systems, Faculty of Engineering, Multimedia University, Cyberjaya, 63100, MALAYSIA*
[3] *Faculty of Electronics and Communication Engineering, NIIT University, Rajasthan, 301705, INDIA*
[4] *NEX Network Edge Group, Intel Corporation, Bayan Lepas, 11900, MALAYSIA*

*Corresponding Author: kychan@mmu.edu.my
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Abstract

Adders are essential parts of digital systems where critical design factors like size, power consumption, and latency are critical. This work presents a single-bit full adder based on the Modified Gate Diffusion Input (MGDI) technique to enhance the efficiency of these parameters. Extensive simulations were conducted using Mentor Graphics and 130nm CMOS technology, with extensive analysis comparing the proposed adder's performance against a standard CMOS adder across different voltage supply levels. The proposed adder utilizes only 8 transistors, significantly fewer than the 28 transistors required in conventional CMOS full adders. The MGDI technique proves highly effective, reducing power dissipation by 98.8%, area consumption by 18.1%, and propagation delay by 86.1%, while also simplifying circuit complexity. The suggested adder continuously exhibits decreasing power consumption and shorter propagation delay as the supply voltage rises, highlighting its appropriateness for high-performance, low-power applications. The reduced transistor count and minimized wiring complexity further establish the proposed adder as a compelling alternative to traditional CMOS designs.

1. Introduction

The method of building an integrated circuit (IC) by joining and integrating transistors on a single chip to accomplish particular functions is known as Very-Large-Scale Integration, or VLSI. In VLSI design, area, performance, functionality, and reliability are crucial factors. VLSI designers have been concentrating more on speed, area, and power consumption optimization in the past several years.

Due to its excellent noise immunity and low static power dissipation, complementary metal-oxide-semiconductor (CMOS) technology—which combines N-Channel and P-Channel metal-oxide-semiconductor (PMOS) transistors—is frequently employed in digital circuit design. Power dissipation is greatly reduced since PMOS and NMOS transistors are complementary, meaning that one transistor is always off during state changes. Two factors affect the amount of power consumed in CMOS circuits: static and dynamic dissipation. Subthreshold conduction while transistors are off, leakage current through reverse-biased diodes, and tunneling current

through gate oxide are the causes of static dissipation. Conversely, short-circuit pathways and load capacitance are the sources of dynamic power dissipation [1].

Pull-up and pull-down networks work together to power CMOS logic. Based on these networks' activity, internal capacitance charges and discharges occur. Pull-up and pull-down networks are complementary in digital CMOS circuits, which means that one is active while the other is dormant [2]. This arrangement ensures that CMOS only consumes power during switching events, known as dynamic power dissipation. In contrast, NMOS logic circuits consume power even in idle mode. Traditionally, chip design focused primarily on speed and area. However, with the increasing power density, reducing power consumption has become a key consideration in CMOS chip design.

Pass Transistor Logic (PTL) is another method utilized in circuit construction besides CMOS. PTL uses NMOS and PMOS transistors to switch and pass logic levels between nodes, hence reducing the number of transistors and power consumption. However, voltage levels may degrade at each stage, requiring the restoration transistors to maintain output integrity. When the gate input is high, NMOS transistors are arranged in series or parallel close, passing a weak '1' and a strong '0'. When the gate input is low, a similar arrangement of PMOS transistors closes, passing a weak '0' and a strong '1' [3].

The advantages of PTL over CMOS include: (i) No static leakage, (ii) Reduced switching capacitance, (iii) Efficient handling of short-circuit power, and (iv) Lower switching activity through transistor sizing and glitch elimination [4]. Two NMOS transistors, two output inverters for complementary signals, and two tiny pull-up PMOS transistors for swing restoration are all part of complementary pass transistor logic, or CPL. Although CPL has some advantages, including low input capacitance, minimal internal voltage swing, and strong output driving capacity, a major disadvantage is that it necessitates the use of two MOS networks [5].

In CMOS logic circuits, the Gate Diffusion Input (GDI) technique is applied. It comprises three inputs: an output, an input to the source of NMOS (N), an input to the source of PMOS (P), and a common gate input of NMOS and PMOS (G). The NMOS and PMOS transistors' bodies are linked to their corresponding sources. Fig. 1 depicts a GDI cell. Numerous functions of the cell can be confirmed by applying logic signals to the inputs. Table 1 lists some of the functionalities achievable with the GDI cell, many of which are complex to implement using standard CMOS or PTL. The GDI technique requires only two transistors per function, offering a significant advantage [6].

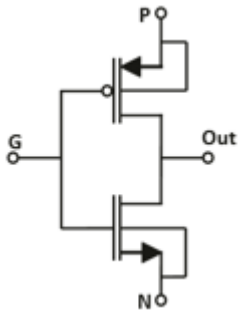

Fig. 1 *The GDI Cell*

Table 1 *The functions of a GDI cell*

G	N	P	Function	Output
A	0	B	F1	$\bar{A}$ B
A	B	1	F2	$\bar{A}$ + B
A	1	B	OR	A + B
A	B	0	AND	AB
A	C	B	MUX	$\bar{A}$B + AC
A	0	1	NOT	$\bar{A}$

The threshold voltage drop, which lowers current and affects the gate's resolution, is the main disadvantage of the GDI gate. Swing restoration buffers at the output might be used to make up for this drop in output voltage. Swing deterioration and fabrication complexity brought on by body connections are further issues with GDI that can be avoided by utilizing Modified Gate Diffusion Input (MGDI) logic [6].

A GDI cell and an MGDI cell share a similar basic structure. As illustrated in Fig. 2, the PMOS and NMOS bodies in MGDI are connected to VDD and Ground, respectively. This configuration provides constant body biasing, enhancing circuit stability and reducing loading effects. MGDI is particularly well-suited for designing high-performance logic circuits, offering advantages such as fewer transistors, improved swing degradation, and better

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static power characteristics compared to other techniques like Complementary Pass Transistor Logic (CPL), Static CMOS, and Pass Transistor Logic (PTL).

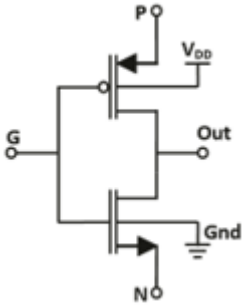

Fig. 2 *The MGDI Cell*

The wiring complexity, size, speed, and power consumption of a circuit are all greatly impacted by the logic style selection. Factors such as operating conditions, suitability, and transistor scaling affect the logic style employed in system circuits [7]. In this paper, the key parameters under consideration include delay, power dissipation, and circuit size. The single-bit half adder and full adder, which are core components, will be designed using MGDI cells [8]. Two input signals (A and B) and two output signals (SUM and CARRY) make up the single-bit half adder. The characteristic equations are as follows.

$$SUM = AB^* + A^*B = A \oplus B \quad (1)$$

$$CARRY = AB \quad (2)$$

The single-bit full adder is a combinational circuit that generates the matching SUM and CARRY by doing the arithmetic sum of the three bits, A, B, and Cin. The following is the expression for the characteristic equations of the full adder's SUM and CARRY equations.

$$SUM = A \oplus B \oplus Cin \quad (3)$$

$$CARRY = A.B + A.Cin + B.Cin \quad (4)$$

$$CARRY = A.B + Cin.(A \oplus B) \quad (5)$$

$$CARRY = A.(\overline{A \oplus B}) + Cin.(A \oplus B) \quad (6)$$

A MGDI cell designed standard logic gates library will be designed. The half adder and full adder will also be designed using MGDI. The following of this paper is presented as follows. The detailed transistors level circuit diagrams will be discussed in section 2. Extensive simulation results and analyses will be presented in section 3. Finally, a conclusion will be drawn in the last section.

2. Circuit Design Using Modified Gate Diffusion Input (MGDI) Technique

The design process was conducted using Design Architect-IC by Mentor Graphics, utilizing the TSMC (Taiwan Semiconductor Manufacturing Company) 130 nm CMOS technology. The transistor dimensions were defined with a fixed length of 0.13 µm, and the width was adjusted according to the specific requirements of the circuitry. To create the schematic for the full adder in Design Architect-IC, the process began by identifying and defining the necessary logic gates, including the inverter, AND gate, multiplexer, and XOR gate. These logic gates were designed and simulated at the transistor level, which was then followed by the integration of these components to construct the full adder.

2.1 Transistor-Level Circuit Design of Standard Logic Gates Using MGDI Technique

A basic digital logic gate with one input and one output that performs logical negation on its input is an inverter, sometimes referred to as a NOT gate. Fig. 3 shows the schematic of an inverter utilizing the Modified Gate Diffusion Input (MGDI) approach. Table 2 describes the transistor operations that correspond to this inverter. Another fundamental digital logic gate that accomplishes the logical conjunction is the AND gate, which has an output of 0 unless all of the inputs are 1. While a conventional CMOS AND gate typically uses 8 transistors, the MGDI technique allows the design of an AND gate using just two transistors, as shown in the schematic in Fig. 4, with the transistor operations outlined in Table 3.

A 2-to-1 multiplexer, which has three inputs (A, B, and a selector) and one output, selects one of the inputs to pass through to the output based on the selector's state. The standard CMOS 2-to-1 multiplexer uses 6 transistors,

but the MGDI technique reduces this to only 2 transistors, as depicted in the schematic in Fig. 5, with operations summarized in Table 4.

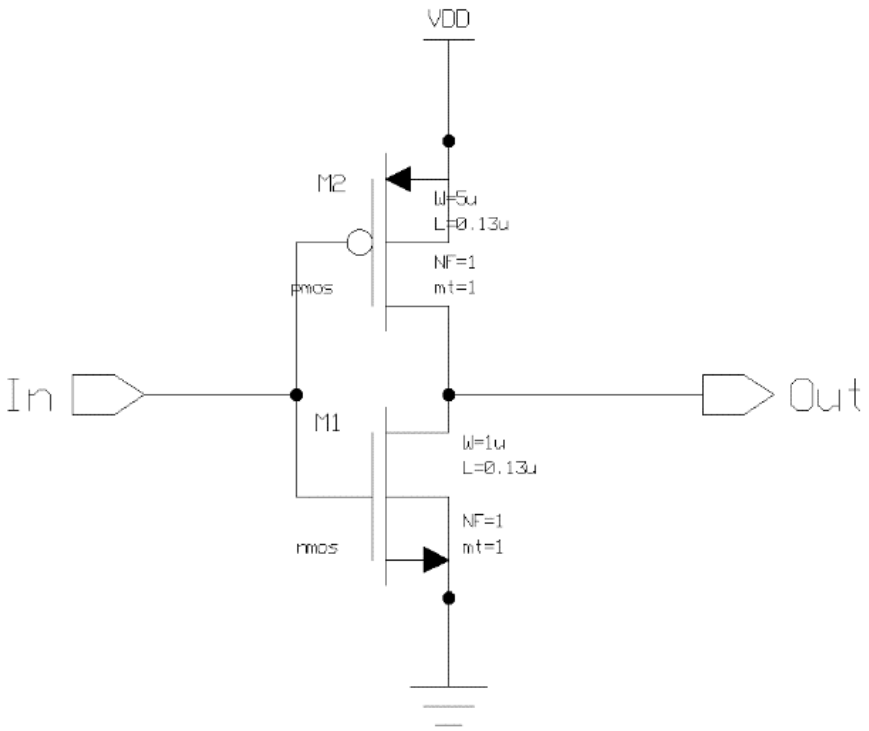

Fig. 3 *The schematic of the Invertor using MGDI*

Table 2 *The truth table of the Invertor using MGDI*

In	M1	M2	Out
0	OFF	ON	1
1	ON	OFF	0

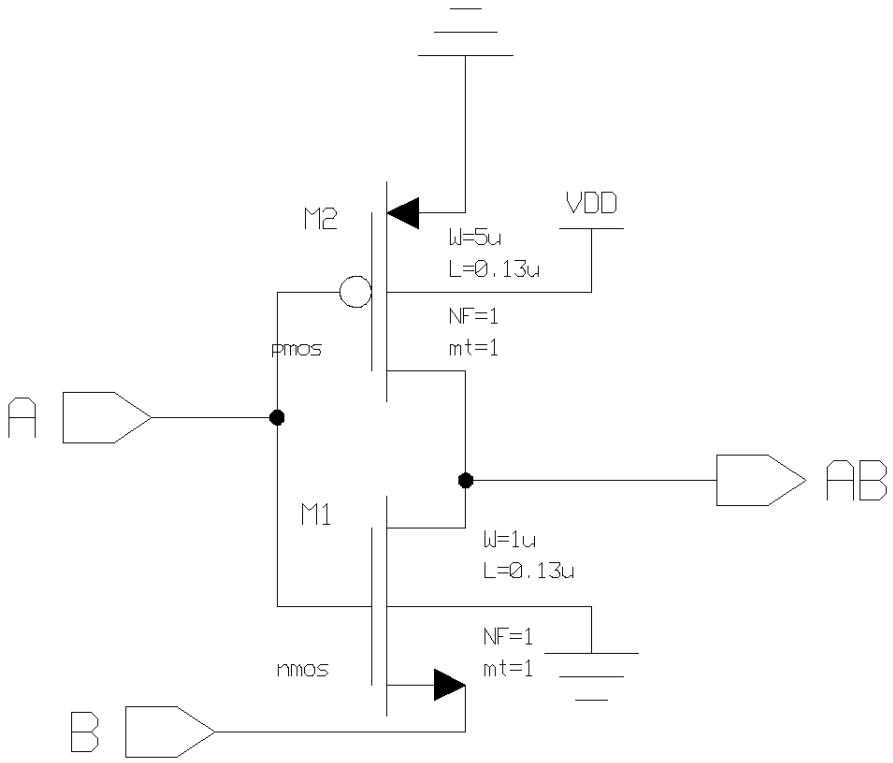

Fig. 4 *The schematic of the AND using MGDI*

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Table 3 *The truth table of the AND using MGDI*

A	B	M1	M2	Out
0	0	OFF	ON	0
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	1

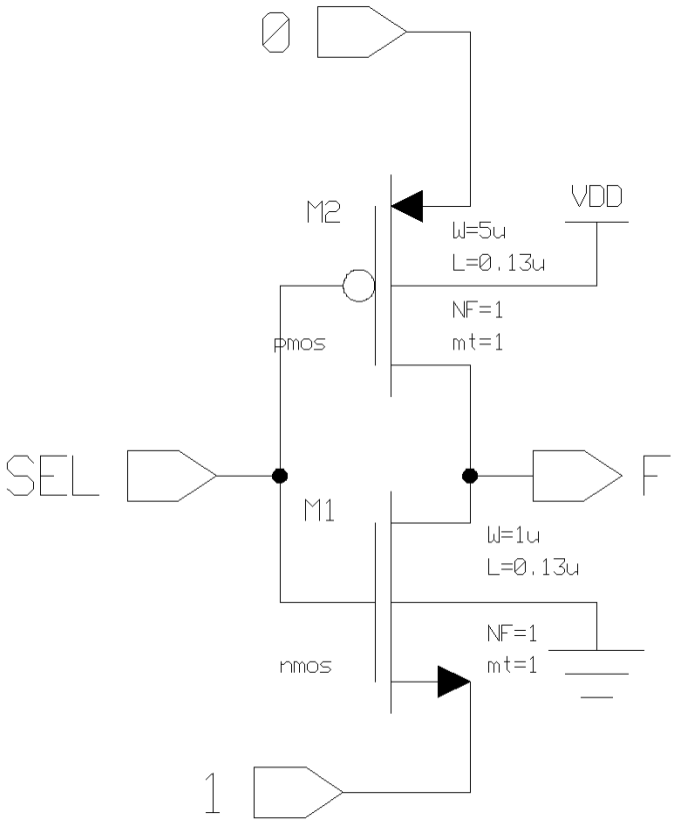

Fig. 5 *The schematic of the 2-to-1 multiplexer using MGDI*

Table 4 *The truth table of the 2-to-1 multiplexer using MGDI*

SEL	M1	M2	Out
0	OFF	ON	A
1	ON	OFF	B

The XOR gate, which performs the exclusive OR operation, outputs a HIGH signal if the inputs are different and a LOW signal if they are the same. A conventional CMOS XOR gate requires 8 transistors, but the MGDI technique reduces this number to 4 transistors, as shown in Fig. 6, with the corresponding operations detailed in Table 5. Furthermore, an enhanced version of the XOR gate is proposed, combining the MGDI and Pass Transistor Logic techniques. This hybrid approach reduces the number of transistors further to just 3, effectively decreasing both delay and power dissipation. The schematic of the enhanced 3-transistor XOR gate is shown in Fig. 7, with its truth table presented in Table 6.

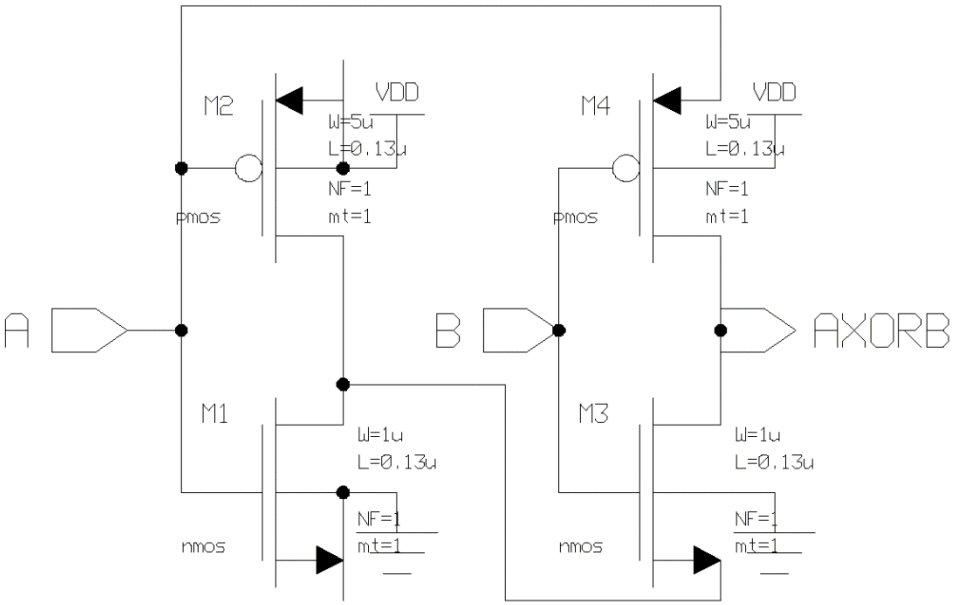

Fig. 6 *The schematic of the XOR using MGDI*

Table 5 *The truth table of the XOR using MGDI*

A	B	M1	M2	M3	M4	AXORB
0	0	OFF	ON	OFF	ON	0
0	1	OFF	ON	ON	OFF	1
1	0	ON	OFF	OFF	ON	1
1	1	ON	OFF	ON	OFF	0

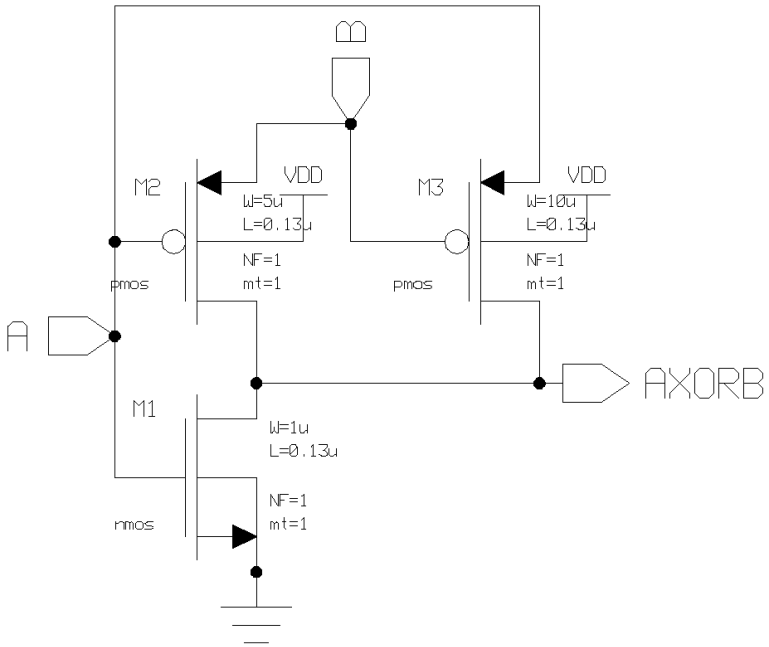

Fig. 7 *The schematic of the enhanced 3-transistor XOR*

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Table 6 *The truth table of the enhanced 3-transistor XOR*

A	B	M1	M2	M3	AXORB
0	0	OFF	ON	ON	0
0	1	OFF	ON	OFF	1
1	0	ON	OFF	ON	1
1	1	ON	OFF	OFF	0

2.2 Transistor-Level Circuit Design of the Full Adder

The CMOS Full Adder is constructed using Pull-Up and Pull-Down Networks, comprising 28 transistors based on the Boolean logic expressions of the sum equation (3) and carry equation (5). The schematic of this complementary CMOS full adder, as depicted in Fig. 8, includes 12 transistors dedicated to generating the carry output and 16 transistors responsible for producing the sum output from the inverted carry signal. Due to this structure, the propagation delay for the sum is noticeably higher than that for the carry, leading to increased power consumption and dissipation.

The enhanced 8-transistor MGDI Full Adder, depicted in Fig. 9, presents a highly efficient design with only 8 transistors compared to traditional approaches. The transistor operations for this adder are detailed in Table 7, which describes the interaction of the three input signals (A, B, and Cin) with the two output signals (Carry, C, and Sum, S). This design leverages an enhanced 3-transistor XOR gate, introduced in the previous section, to generate the Sum output. Additionally, the Carry output is generated using a 2-to-1 multiplexer, designed with the MGDI technique and based on equation (6). By streamlining the transistor count, this design achieves significantly lower power consumption and enhanced efficiency, making it a superior choice for modern digital circuits.

Table 7 *The truth table of the 8-transistor MGDI Full Adder*

A	B	Cin	M1	M2	M3	M4	M5	M6	M7	M8	C	S
0	0	0	OFF	ON	ON	OFF	ON	ON	OFF	ON	0	0
0	0	1	OFF	ON	ON	OFF	ON	OFF	OFF	ON	0	1
0	1	0	OFF	ON	OFF	ON	OFF	ON	ON	OFF	0	1
0	1	1	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	1	0
1	0	0	ON	OFF	ON	ON	OFF	ON	ON	OFF	0	1
1	0	1	ON	OFF	ON	ON	OFF	OFF	ON	OFF	1	0
1	1	0	ON	OFF	OFF	OFF	ON	ON	OFF	ON	1	0
1	1	1	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	1	1

2.3 Layout Design Using Modified Gate Diffusion Input (MGDI) Technique

The layout design of an integrated circuit provides a detailed three-dimensional arrangement and interconnection of its elements before fabrication. Prior to creating the layout, the schematic design was thoroughly developed to ensure the circuit's proper functionality. In this study, circuit routing was achieved using various metal layers, with polysilicon (poly) serving as the fundamental bridge for connections. Metals were primarily used to link sources, drains, inputs, and outputs, establishing the circuit's conduction paths, while poly was utilized for gate connections. Additional components such as vias, poly contacts, p-wells, and n-wells were integrated to complete the overall connectivity.

The layout design was conducted separately for each circuit element, utilizing Metal 1 and Metal 2 layers to establish connection points. The physical verification process was carried out using the EDA Mentor Graphics tool, beginning with a Design Rule Check (DRC) to ensure compliance with design rules, such as spacing and minimum dimensions. This step was meticulously performed for every component to verify adherence to the required standards. Following the DRC, a Layout Versus Schematic (LVS) check was conducted to detect any mismatches between the layout and the schematic design (with DRC and LVS reports included in the appendix).

Finally, Parasitic Extraction (PEX) was employed to extract parasitic components such as resistance and capacitance, which could impact circuit performance. The layout designs for the logic gates, including the inverter, AND gate, 2-to-1 multiplexer, MGDI XOR gate, and the enhanced 3-transistor XOR gate, are illustrated in Fig. 10 through 14. The layouts for the CMOS full adder and the enhanced 8-transistor full adder are presented in Fig. 15 and 16, respectively.

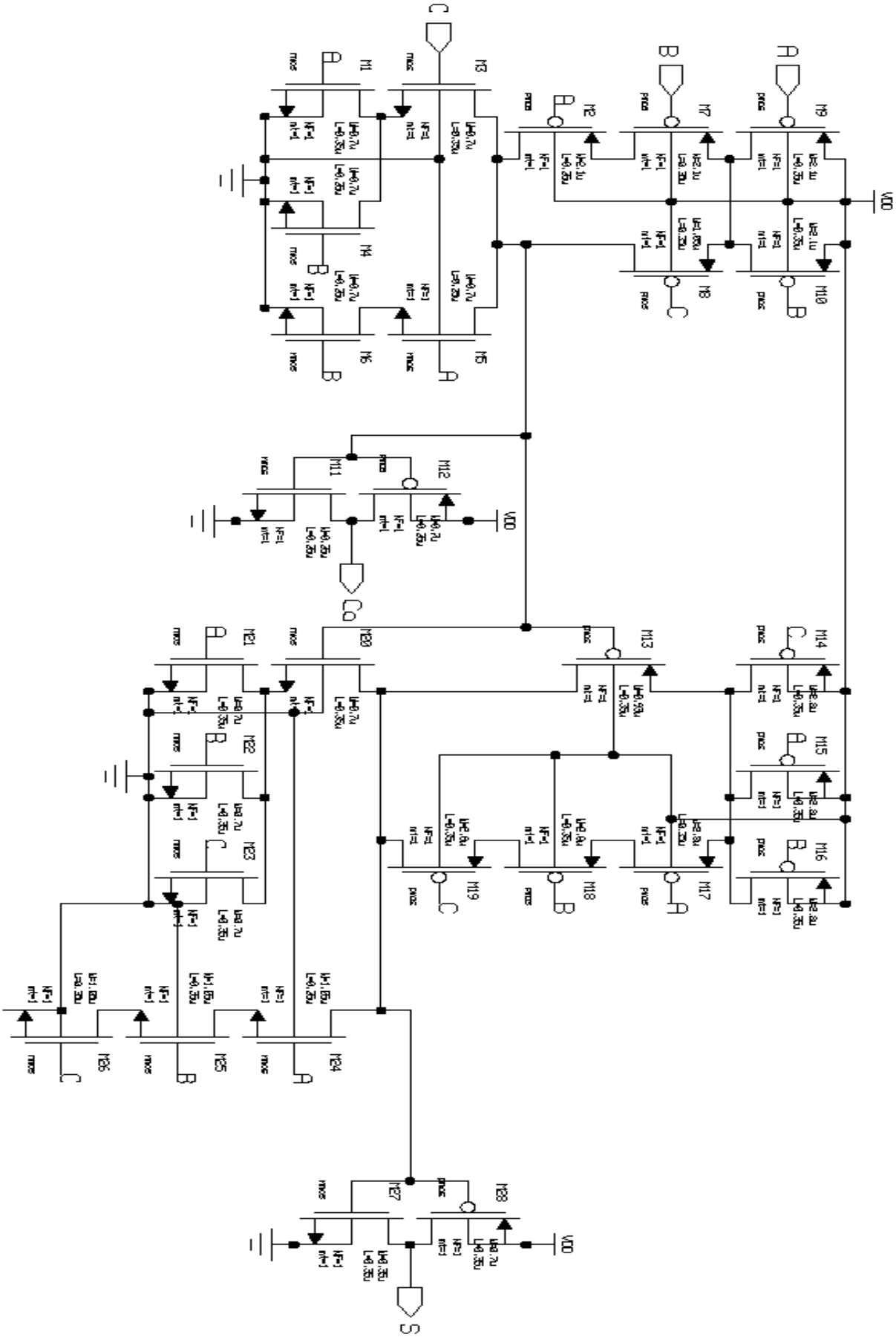

Fig. 8 *The schematic of the original CMOS Full Adder*

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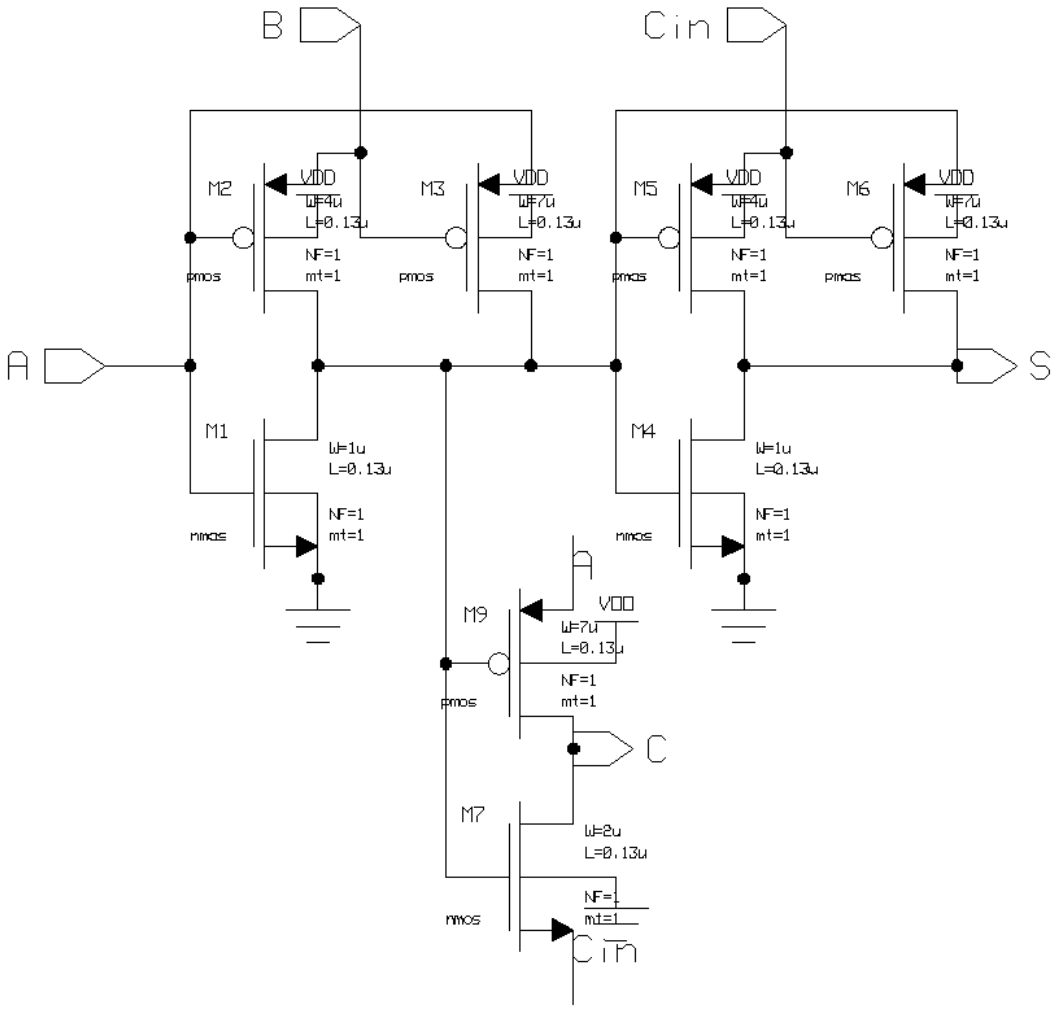

Fig. 9 *The schematic of the enhanced 8-transistor MGDI Full Adder*

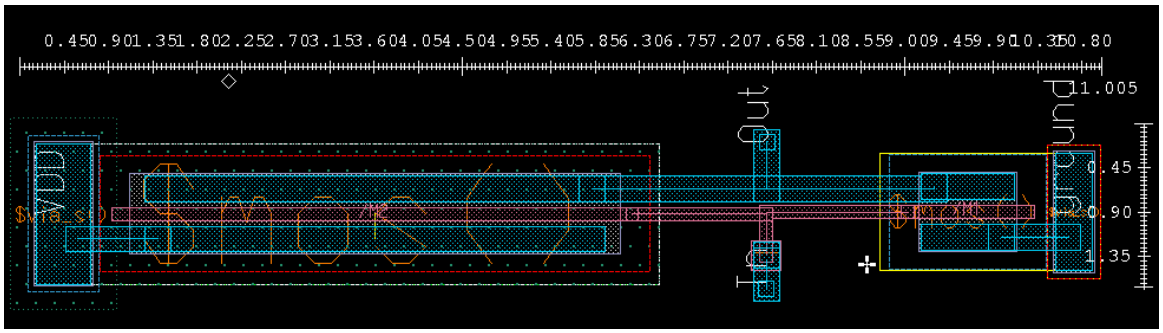

Fig. 10 *The layout of the inverter*

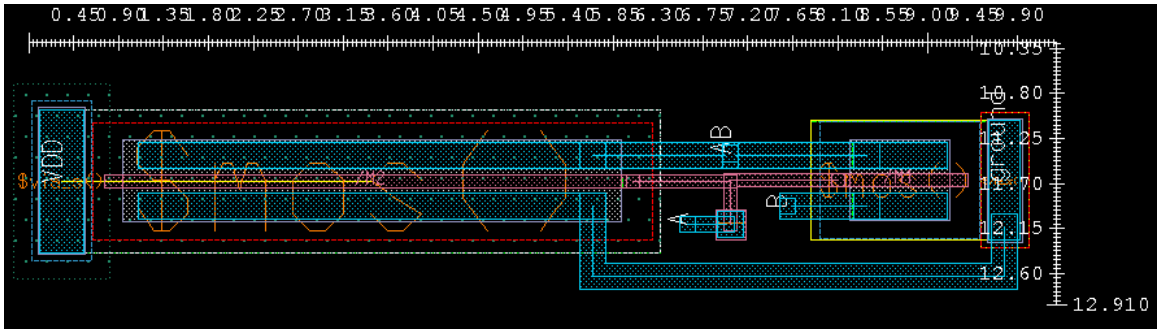

Fig. 11 *The layout of the GDI AND gate*

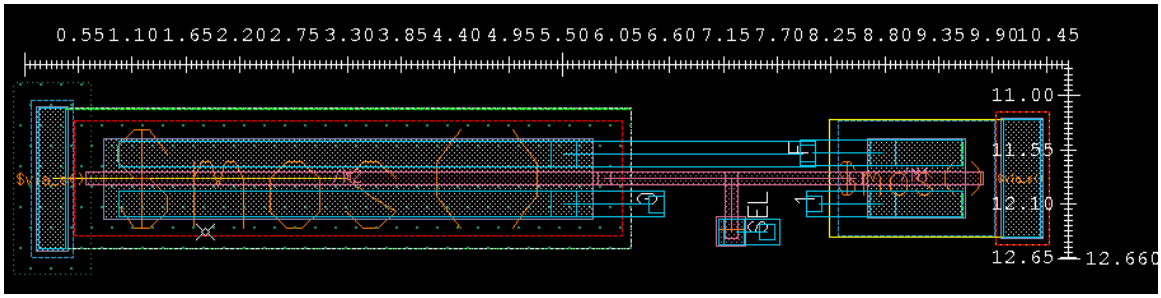

Fig. 12 *The layout of the 2-to-1 multiplexer*

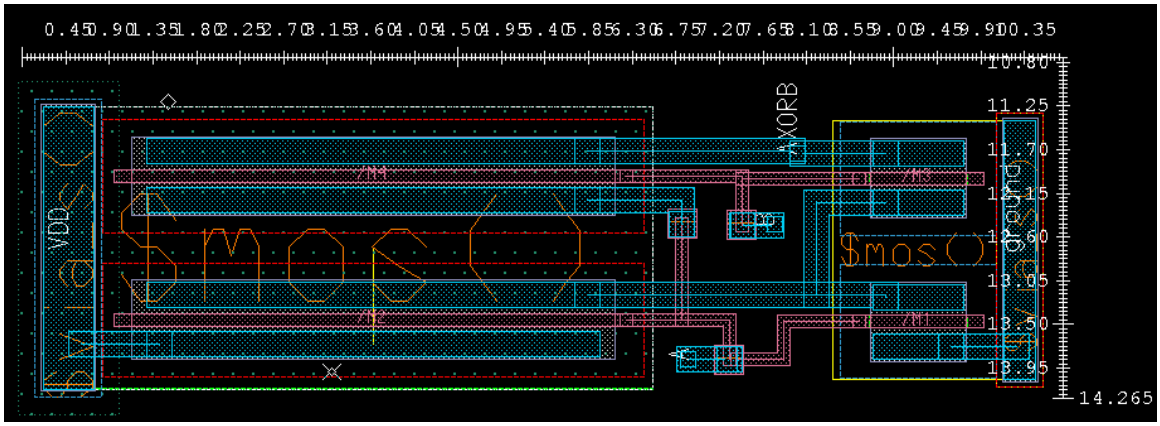

Fig. 13 *The layout of the GDI XOR gate*

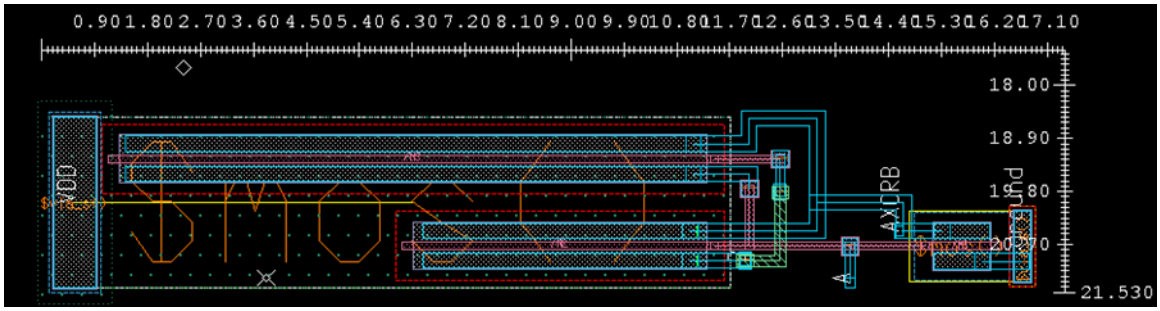

Fig. 14 *The layout of the enhanced 3-transistor XOR gate*

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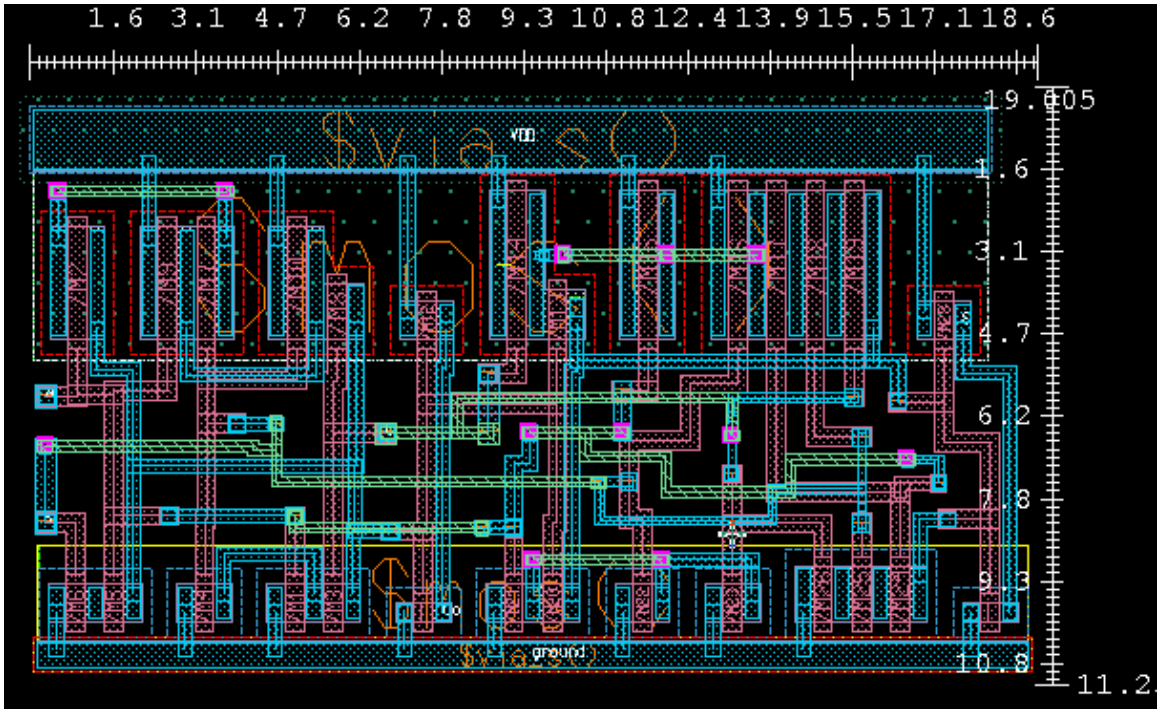

Fig. 15 *The layout of the CMOS full adder*

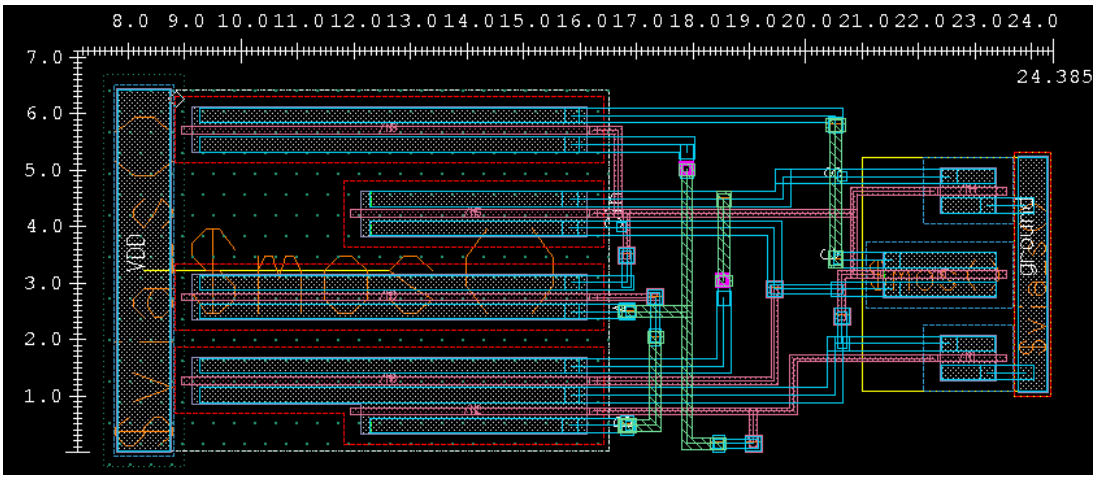

Fig. 16 *The layout of the enhanced 8 transistors full adder*

3. Simulation Results and Analysis

Parasitic Extraction (PEX) is performed after successfully passing the LVS (Layout Versus Schematic) check. PEX identifies and extracts parasitic resistance and capacitance from the completed circuit layout. This information is then used in post-layout simulations to verify that the design operates within the specified parameters. The parasitic extraction in this case is simulated at a supply voltage of 0.8V under room temperature condition.

Fig. 17 displays the simulation waveforms of an inverter. The output, V(OUT), is the inverse of the input, also a square wave but with opposite polarity. Key performance metrics include a delay of 2.5935 ns, a rise time of 4.3516 ns, and a fall time of 4.3516 ns. Fig. 18 depicts the simulation waveforms of an AND gate. The output, V(OUT), follows the AND logic function, producing a high output only when both inputs are high. Key performance indicators include a delay of 2.0851 ns and a rise time of 30.545 ns, which determine the gate's speed and responsiveness. Fig. 19 displays the simulation waveforms of a 2-to-1 multiplexer. The output, F, accurately reflects the multiplexer's function, selecting either A or B based on the select, SEL signal. The delay of 146.65 ps indicates the time it takes for the output to respond to changes in the inputs or select signal. The inverter exhibits the shortest delays and fastest rise/fall times due to their simple structure. AND gate typically introduce slightly longer delays and rise/fall times compared to inverter. The 2-to-1 multiplexer, being more complex components, often has the highest delays among these three.

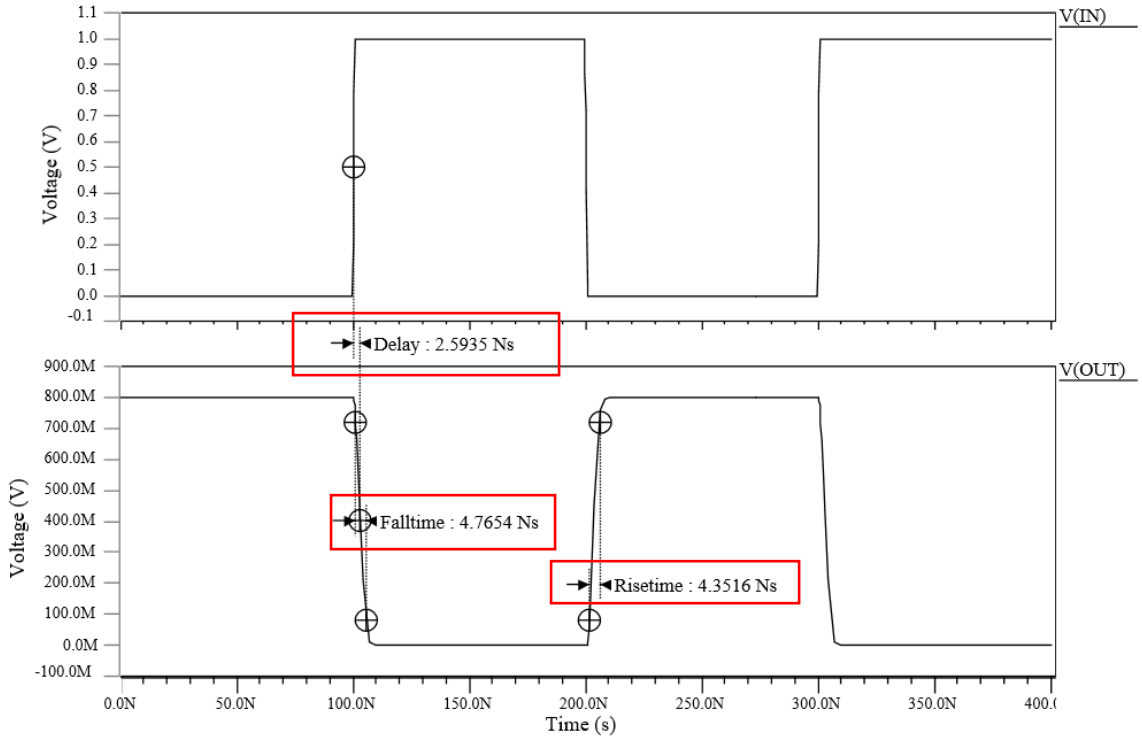

Fig. 17 *The simulation waveforms of the inverter*

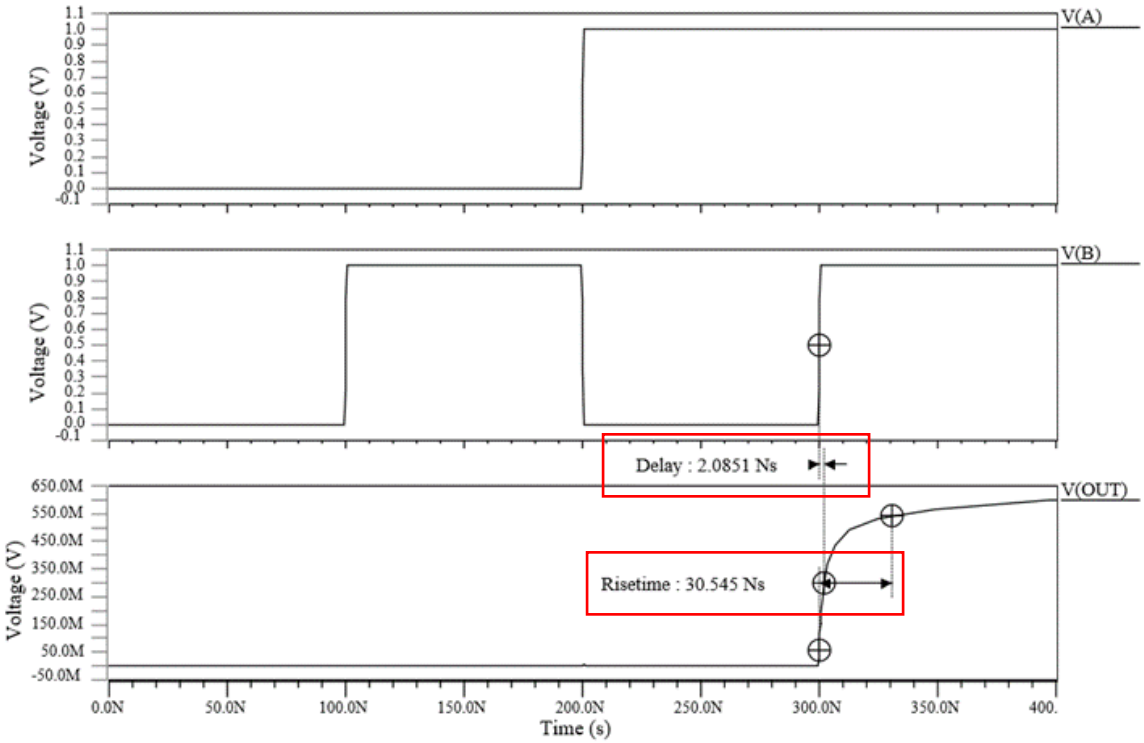

Fig. 18 *The simulation waveforms of the AND gate*

Fig. 20 illustrates the simulation waveforms of the MGDI XOR gate. The input signals, A and B, exhibit clear square wave patterns. The output, V(OUT), accurately reflects the XOR logic function, producing a high output when inputs differ and a low output when inputs are identical. However, the MGDI XOR gate suffers from relatively long propagation delay (38.318 ns) and rise time (101.69 ns), limiting its overall speed.

In contrast, Fig. 21 presents the simulation waveforms of the enhanced 3-transistor XOR gate. The input waveforms, A and B, remain similar to the MGDI XOR gate. The output, V(OUT), likewise adheres to the XOR logic function. The critical difference lies in the timing parameters. The enhanced 3-transistor XOR gate exhibits

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substantially reduced propagation delay (3.196 ns) and rise time (6.141 ns) compared to the MGDI XOR gate. These improvements translate to faster switching speeds and higher operational frequency, making it a more suitable choice for high-performance digital circuits. It clearly demonstrates the performance advantage of the enhanced 3-transistor XOR gate. The reduced propagation delay (91.65%) and rise time (93.96%) evident in Fig. 21 enable faster signal transitions, as opposed to the longer delay observed in Fig. 20. This performance enhancement is attributed to the optimized circuit design of the enhanced 3-transistor XOR gate, which effectively minimizes internal signal paths and reduces capacitive loading. As a result, the enhanced 3-transistor XOR gate is a preferred choice for applications demanding high-speed operation and low power consumption.

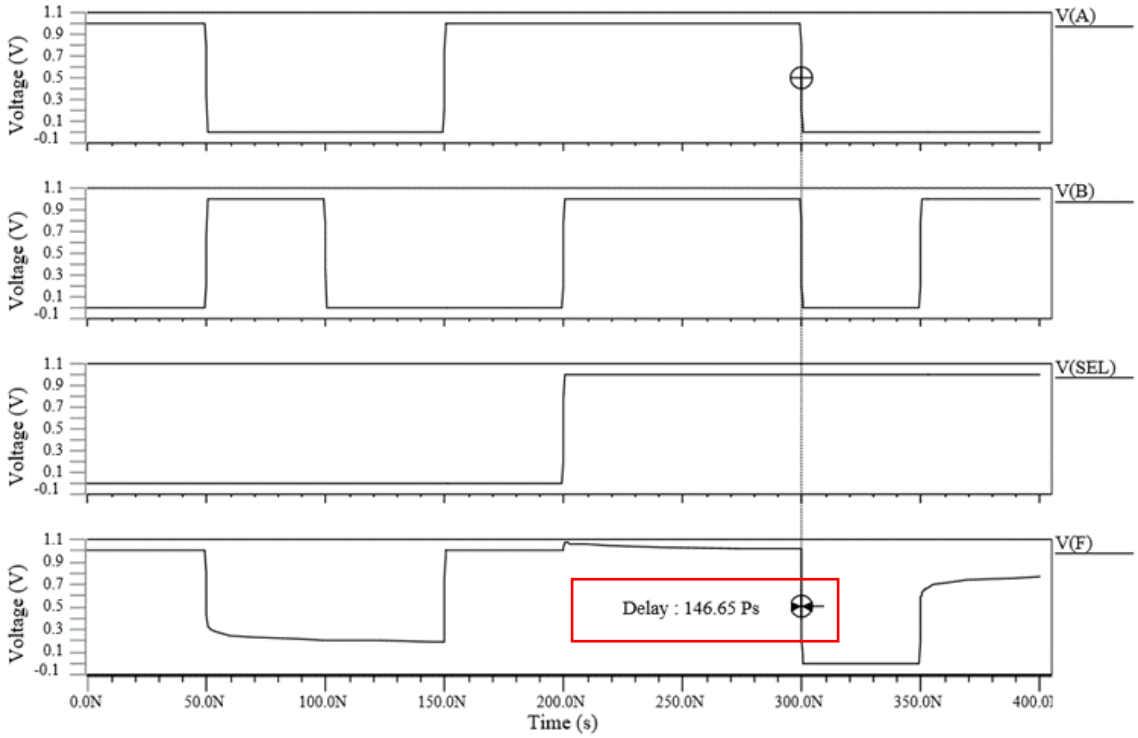

Fig. 19 *The simulation waveforms of the 2-to-1 multiplexer*

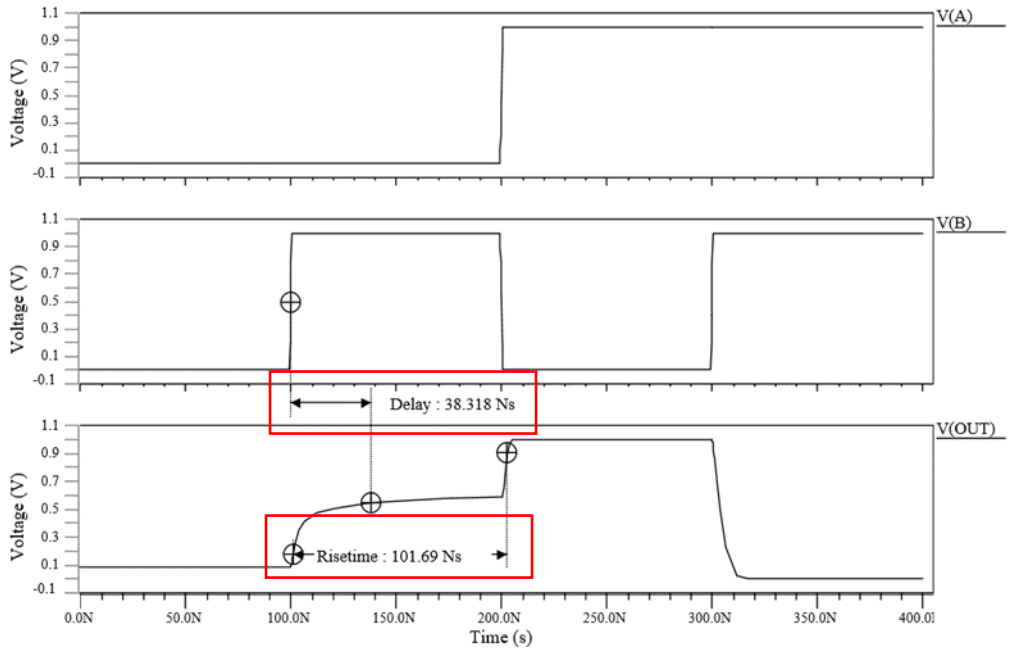

Fig. 20 *The simulation waveforms of the GDI XOR gate*

The simulation results of the 8-transistor full adder and the CMOS full adder reveal significant differences in their performance, particularly in terms of delay and power efficiency. The waveforms from the 8-transistor full

adder, as shown in Fig. 23, demonstrate that this design is highly efficient with respect to speed. The Sum output has a remarkably low delay of 1.6526 ns, while the Carry output exhibits a slightly higher delay of 7.3478 ns. This difference in delay times between the Sum and Carry outputs suggests that while the 8-transistor design is fast, it may still require some optimization for the Carry output. Additionally, the rise and fall times for the Sum output are 152.94 ps and 157.25 ps, respectively, indicating a symmetric switching behavior. However, the Carry output shows larger rise and fall times, 10.971 ns and 19.628 ns, respectively, pointing to a slower response time, which is expected given the reduced number of transistors in this design.

In contrast, the CMOS full adder, illustrated in Fig. 22 presents a much higher delay in both the Sum and Carry outputs. The Sum output exhibits a delay of 76.601 ns, while the Carry output shows a delay of 52.771 ns. These delay times are significantly higher than those observed in the 8-transistor full adder, indicating that the CMOS design is less efficient in terms of speed. The increased complexity of the CMOS full adder, due to the higher number of transistors, contributes to these larger delay times, making it less suitable for applications where rapid signal processing is essential.

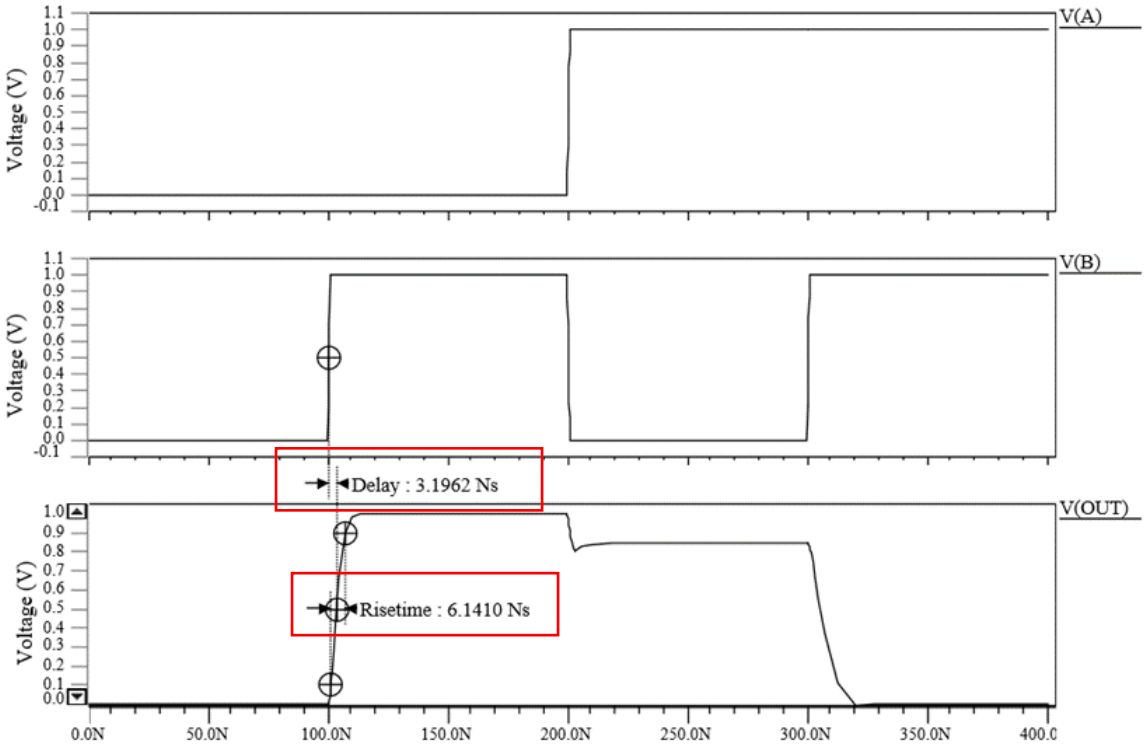

Fig. 21 *The simulation waveforms of the enhanced 3-transistor XOR gate*

Table 8 details the power consumption and delay metrics for various digital circuits, revealing several critical insights. The inverter circuit, for instance, exhibits a power consumption of 478.7 pW and a delay of 2.5935 ns, which are typical values for such a fundamental component. The AND gate stands out with the lowest power consumption at 1.58 pW and a delay of 2.0851 ns, highlighting the efficiency of its simple operation. Meanwhile, the 2-to-1 multiplexer, although consuming a higher power of 671.88 pW, achieves an exceptionally low delay of 0.14665 ns, making it well-suited for speed-critical applications. The MGDI XOR gate, however, shows a higher power consumption of 500.12 pW paired with a significant delay of 38.318 ns, indicating a potential performance bottleneck due to the inherent complexity of XOR operations. On the other hand, the enhanced 3-transistor XOR gate demonstrates substantial improvements, with a drastically reduced power consumption of just 2.65 pW and a much lower delay of 3.1962 ns, showcasing the effectiveness of its design modifications. The CMOS full adder, while consuming 516.008 pW, suffers from a substantial delay of 76.601 ns, suggesting limitations in its speed efficiency for high-performance applications. Lastly, the 8-transistor full adder achieves a notable reduction in power consumption to 6.4 pW, albeit with a delay of 7.3478 ns, reflecting a deliberate trade-off favoring power efficiency over speed.

When comparing the two designs, it becomes evident that the 8-transistor full adder is more efficient, particularly in high-speed applications. Its lower delay times (97.84% for Sum and 86.08% for Carry) and reduced power consumption make it an attractive option for scenarios where performance and energy efficiency are critical. Conversely, the CMOS full adder, while less efficient in terms of speed, may offer advantages in terms of noise immunity and robustness, making it more suitable for applications where these factors are more critical

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than speed. Overall, the 8-transistor full adder, utilizing the MGDI, offers a significant performance improvement over the traditional CMOS full adder, particularly in terms of speed and power efficiency.

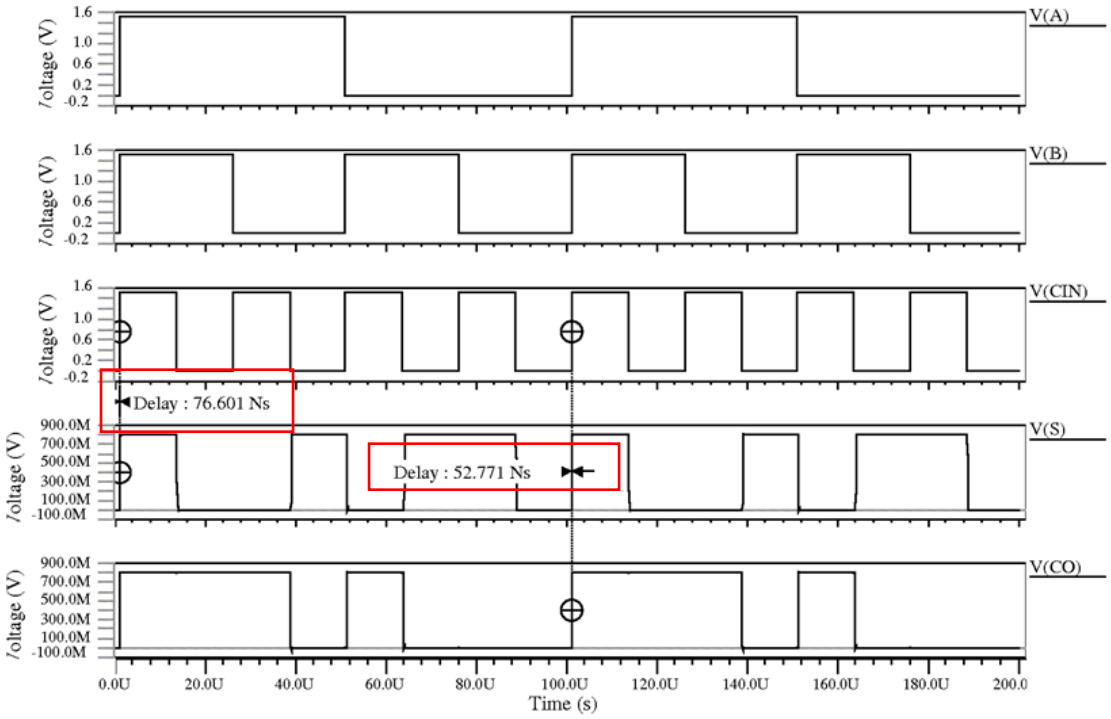

Fig. 22 *The simulation waveforms of the CMOS full adder*

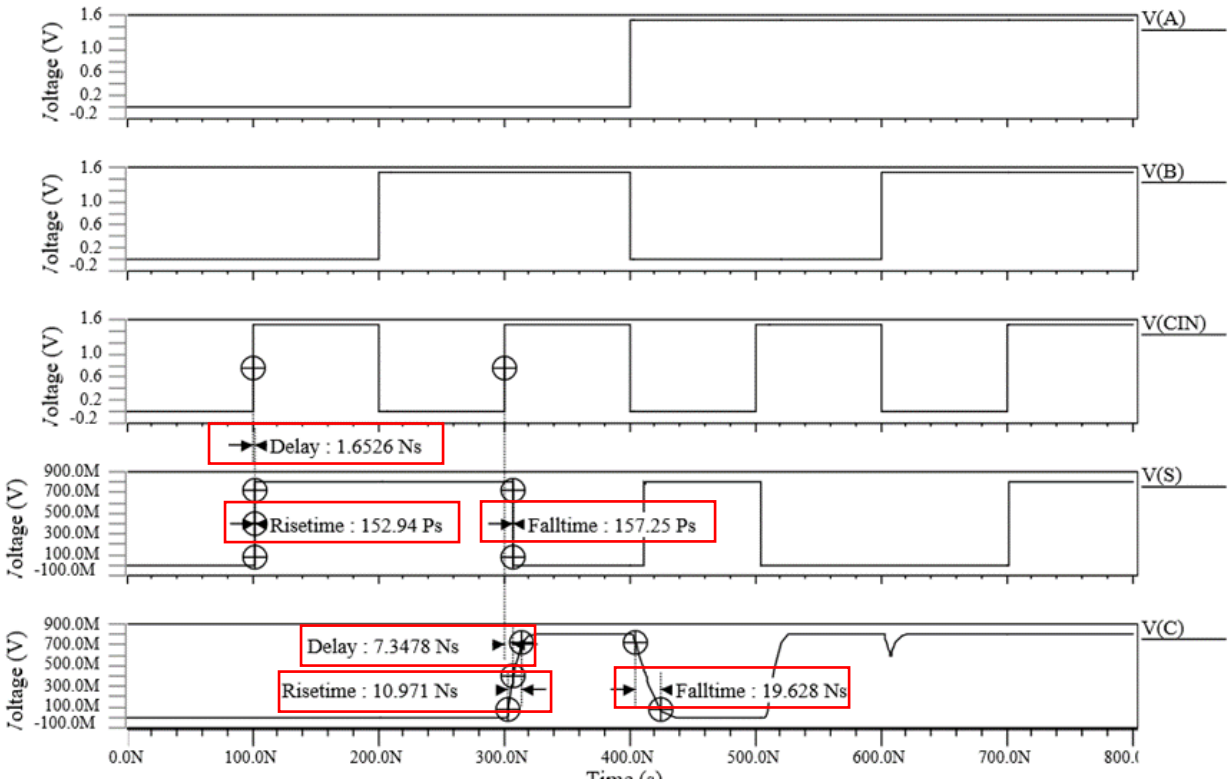

Fig. 23 *The simulation waveforms of the 8 transistors full adder*

Table 9 offers a direct comparison between the CMOS full adder and the enhanced 8-transistor full adder at a supply voltage of 0.8V. The enhanced design significantly reduces the transistor count to just 8, compared to 28 in the CMOS full adder, contributing to lower power consumption and simplified circuit complexity. This reduction in components directly correlates with the enhanced full adder's dramatically lower power dissipation of 6.40

pW, a stark contrast to the 516.01 pW consumed by the CMOS design. It boasts a remarkable 98.76% reduction in power consumption, demonstrating exceptional power efficiency. Moreover, the Sum delay in the enhanced 8-transistor full adder is reduced to 1.626 ns, a substantial improvement over the CMOS full adder's 76.601 ns, demonstrating the enhanced design's superior speed performance. Similarly, the Carry delay is also markedly lower in the enhanced design at 7.347 ns, compared to 52.771 ns in the CMOS full adder. It accelerates performance with a 97.88% improvement in sum delay and a notable 86.08% reduction in carry delay. These further reinforce the efficiency gains achieved through the MGDI technique.

Table 8 *The power consumption and delay of the circuit designed*

Circuit	Power (pW)	Delay (ns)
Inverter	478.7	2.5935
AND	1.58	2.0851
2-to-1 multiplexer	671.88	0.14665
XOR	500.12	38.318
Enhanced XOR	2.65	3.1962
CMOS full adder	516.008	76.601
Enhanced 8 transistors full adder	6.4	7.3478

Table 9 *The performance of CMOS full adder versus enhanced 8 transistors full adder proposed*

Voltage supply = 0.8V	Number of transistors	Power dissipation (pW)	Sum Delay (ns)	Carry Delay (ns)
CMOS full adder	28	516.01	76.601	52.771
8 transistors full adder	8	6.40	1.626	7.347
Percentage improvement (%)	71.4	98.8	97.9	86.1

Table 10 *The power consumption and delays of the enhanced 8 transistors full adder under various voltage supply values*

Voltage supply	0.6V	0.8V	1.2V
Power (pW)	3.341	6.405	14.520
Sum_Delay (ns)	8.231	1.626	1.231
Carry_Delay (ns)	12.512	7.347	5.831

Table 11 *The comparison of the power consumption between the enhanced 8 transistors full adder with the existing full adders*

Full Adders	Number of Transistors	Power
Gate Diffusion Input-Transmission Gate Adder [9]	18	8.058 mW
Mixed Logic Adder [10]	7	2.070 mW
Hybrid Adder [11]	20	25.800 µW
XOR-XNOR-Based Hybrid Adder [12]	22	0.850 µW
Ripple Carry Adder [13]	9	1.471 µW
Proposed MGDI Adder	8	14.520 pW

Table 10 provides a comprehensive analysis of the enhanced 8-transistor full adder's power consumption and delay metrics across different voltage supply levels. The data reveals that power consumption scales predictably with the voltage supply, increasing from 3.341 pW at 0.6V to 14.52 pW at 1.2V. This behavior is consistent with the expected rise in power usage as the supply voltage increases. Concurrently, the delay for the SUM output improves with higher voltage, decreasing from 8.231 ns at 0.6V to just 1.231 ns at 1.2V, a trend typical of circuits where higher voltage enhances transistor switching speeds. The Carry delay follows a similar pattern, reducing from 12.512 ns at 0.6V to 5.831 ns at 1.2V. The higher delay observed for the Carry output compared to

the Sum output, particularly at lower voltages, suggests that carry generation is more complex and sensitive to voltage variations, requiring careful consideration in low-voltage operations. The enhanced 8-transistor full adder not only achieves higher speed and lower power consumption but also significantly reduces the circuit area by utilizing fewer transistors, thereby minimizing wiring complexity. Table 10 further compares the CMOS full adder with the proposed enhanced 8-transistor full adder, highlighting key differences in transistor count, power consumption, and propagation delay.

In Table 11, a detailed comparison of how well the proposed 8-transistor MGDI adder works and how much power it uses with other recent work is presented. As shown in Table 11, the adder constructed with the transmission gate required 18 transistors and the power consumption is relatively higher compared to the other adders [9]. Another design that used the mixed logic technique that only required 7 transistors has a slightly lower power consumption (2.070 mW) compared to the Gate Diffusion Input-Transmission Gate Adder [10]. The 20 transistors hybrid adder proposed has significantly reduced the power consumption to 25.8 µW [11]. The utilization of XOR-XNOR in the hybrid adder has further reduced the power consumption to 0.850 µW at the cost of an extra 2 transistors compared to the previous design [12]. The Ripple Carry Adder with only 9 transistors successfully reduced the number of transistors needed in the adder with relatively low power consumption (1.471 µW) reported [13]. However, the proposed MGDI 8-transistor full adder outperforms the other adders with the lowest power consumption of 14.520 pW.

The analyses of Tables 8, 9, 10 and 11 clearly underscore the superiority of the enhanced 8-transistor MGDI full adder over traditional CMOS design. In terms of power consumption, delay, and transistor count, the enhanced design consistently outperforms the CMOS full adder, making it a more efficient choice for high-performance, low-power digital circuit applications. The MGDI proves to be highly effective in minimizing power dissipation and reducing delays, especially under varying voltage conditions, positioning the enhanced 8-transistor full adder as a highly attractive option for modern electronic design challenges.

4. Conclusion

In this paper, a full adder is designed using 130 nm technology to enhance performance by reducing power consumption, increasing speed, decreasing complexity, and minimizing circuit size. The design employs an enhanced 3-transistor XOR gate and utilizes the MGDI technique, which excels in lowering power consumption and system complexity compared to alternative methods. By employing fewer transistors, the proposed design reduces the circuit size, with a decrease from 28 transistors in a CMOS full adder to just 8 transistors, achieving a 71.4% reduction in transistor count. This reduction also simplifies wiring complexity. The 8-transistor full adder demonstrates a significant improvement in power consumption, achieving approximately 98.76% reduction, and reduces average propagation delay by about 86.2%. Additionally, the smaller transistor count lowers the chip's temperature, minimizing the need for extensive and costly cooling systems, which in turn reduces the chip's weight, size, and overall lifespan. Enhancing the adder's efficiency can significantly increase digital system performance because addition is a fundamental operation used in many VLSI systems. However, the method's drawback is a lower output voltage. This issue can be addressed by incorporating a buffer to improve output current and resolution.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***study conception and design:*** *Wai Leong Pang, Seyed Arash Zareianjahromi, Swee King Phang;* ***data collection:*** *Seyed Arash Zareianjahromi, Kah Yoong Chan, Angie See Tien Ng;* ***analysis and interpretation of results:*** *Wai Leong Pang, Seyed Arash Zareianjahromi, Kah Yoong Chan;* ***draft manuscript preparation:*** *Kah Yoong Chan, Swee King Phang, Ajay Kumar Singh. All authors reviewed the results and approved the final version of the manuscript.*

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