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A 4x4 Bit Vedic Multiplier with Different Voltage Supply in 90 nm CMOS Technology

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Abstract: In recent years, due to the rapid growth of high performance digital systems, speed and power consumption become very vital in multiplier design. In this paper, a 4x4 bit Vedic multiplier has been designed using the combination of Urdhva Triyakbyam Sutra and 13T hybrid full adder (HFA). This algorithm satisfied the requirement of a fast multiplication operation because of the vertical and crosswise architecture from the Urdhva Triyakbyam Sutra which minimize the number of partial products compared to the conventional multiplication algorithm. The multiplier is simulated using Synopsys Custom Tools with General Process Design Kit (GPDK) of 90 nm CMOS technology using several voltage supplies to find the most optimum value for the voltage supply to be used. The result shows that with the usage of 1 V voltage supply, the new design of multiplier using a combination of HFA and Vedic mathematics is able to produce the lowest power consumption and least delay time. The 4x4 bit Vedic multiplier is able to yield a full output voltage swing with a power consumption of only 0.2015 mW, delay of 376 ps and compact area of 3100 μm^2.

Keywords: voltage supply, multiplier, Vedic mathematics, Low power

1. Introduction

Due to continuous scaling of metal oxide semiconductor (MOS) devices, the number of transistors on single chip increases tremendously. The operating frequency also increases with technology. For this reason, low power design of very large scale integration (VLSI) circuits has been identified and resulted in explosive growth of personal computing devices and wireless communication systems. For applications and systems using microprocessor or digital signal processor, arithmetic logic unit (ALU) is the most important building block in that system [1]. It functions as the core element of complex arithmetic circuits performing addition, multiplication, division, exponentiation, etc. [2]. Out of all these functions, multiplier is the most vital component in processing the signal and adders are the heart of the multiplier [3].

In most of the processors, multiplier manipulates the arithmetic procedure for the improvement of fast processor. A high speed multiplier is able to reduce the delay time and contributes substantially to the total power consumption [4]. In the past, several logic styles have been used to design full adder (FA) cells in multiplier. Although all the adders have similar function, the way of producing the intermediate nodes and the transistor count is varied. Different logic styles tend to favour one performance aspect at the expense of the other. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of the circuit [5].

2. Vedic Multiplier

From various kind of multiplication algorithms available, Vedic algorithm [6] claims to be the most interesting algorithms because it works based on the natural principles on which the human mind works. Vedic mathematics is the name given to the ancient Indian methodology of mathematics that rediscovered by Sri Bharati Krishna Tirthaji in twentieth century [7]. It owned the unique technique of calculation based on the 16 principle which are termed as Sutras [8]. These Sutras covers several modern mathematical terms such as arithmetic, geometry, trigonometry, quadratic equations and factorization. From the 16 Sutras, Urdhva Triyakbhyam Sutra is chosen for doing a multiplication for this project because it is a general multiplication formula applicable to all cases of multiplication [9,10]. Urdhva Tiryakbyham means “vertical and crosswise”. This algorithm satisfied the requirement of a fast multiplication operation because of the vertically and crosswise multiplication concept [11] that adapted well to parallel multiplication process. Hence, it greatly reduces the number of partial products leading to fast multiplication process.

The multiplication algorithm of a 4x4 bit multiplier using Vedic mathematic is described in Table 1. In Table 1, two 4 bit binary numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ are multiplied together and produced 8 bit output $P_7P_6P_5P_4P_3P_2P_1P_0$. The same method can be applied to multiply two binary numbers of any bits (A_N x B_N) with P_N as the product bit.

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Table 1 Multiplication for 4x4 bit Vedic Multiplier

Step	Pictorial Representation	Equations
1	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_0 = A_0*B_0$
2	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_1 = (A_1*B_0) + (A_0*B_1) + \text{Carry}$
3	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_2 = (A_2*B_0) + (A_1*B_1) + (A_0*B_2) + \text{Carry}$
4	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_3 = (A_3*B_0) + (A_2*B_1) + (A_1*B_2) + (A_0*B_3) + \text{Carry}$
5	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_4 = (A_3*B_1) + (A_2*B_2) + (A_1*B_3) + \text{Carry}$
6	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_5 = (A_3*B_2) + (A_2*B_3) + \text{Carry}$
7	$\bullet(A_3)\ \bullet(A_2)\ \bullet(A_1)\ \bullet(A_0)$ $\bullet(B_3)\ \bullet(B_2)\ \bullet(B_1)\ \bullet(B_0)$	$P_6 = A_3*B_3 + \text{Carry}$ $P_7 = \text{Carry}$

Vertical multiplication starts in the first step by taking account of the least significant bit (LSB), A_0 and B_0, giving a product of P_0. Cross multiplication of $A_1 \cdot B_0$ and $A_0 \cdot B_1$ is followed in step 2. The partial products produced from the cross multiplication are summed up to give a product bit of P_1 and a carry. The multiplication is continued in this form until the last vertical multiplication of most significant bit (MSB). The last carry bit from the product produced in step 7 is also known as P_7. Based on these steps, the end result is the final product $P_7P_6P_5P_4P_3P_2P_1P_0$ (8 bit).

3. 4x4 Bit Vedic Multiplier using Urdhva Triyakbhyam Sutra and 13T HFA

From previous research, different techniques had been used to design a multiplier which tends to favour one performance aspect over the other. In hybrid logic style, it utilized more than one module in its circuit design which has benefit over other techniques. Hybrid CMOS design style gives more freedom to designer to select the required modules as well as efficient circuit from different modules for the implementation [12]. Even by optimizing the transistor sizes of the modules it is possible to reduce the delay of all circuits without significantly increasing the power consumption, layout area and possible to achieve least delay [13]. Many full adders can be conceived by using the HFA design style.

In this paper, the multiplier is design using the HFA circuit proposed in [14]. This adder is designed by breaking the full adder into three modules as shown in *Figure 1*. In the previous paper [3], a 2x2 bit Vedic multiplier has been simulated with 3 different types of adders using 1 V power supply. The multiplier with HFA had achieved a low delay time, low power consumption and able to produce output with full swing waveform.

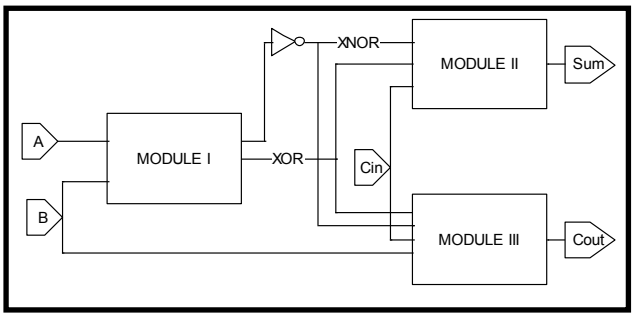

Figure 1 Block Diagram for Hybrid Full Adder

The block diagram of 4x4 bit Vedic multiplier using "Urdhva Triyakbhyam Sutra" is shown in *Figure 2*. This multiplier module is implemented using four input 2x2 bit Vedic multiplier along with three 4 bit ripple carry adders. This design was simulated using General Purpose Design Kit (GPDK) of Synopsys Custom Tools using 90 nm CMOS technology process. The 4x4 bit Vedic multiplier design starts by designing and simulating different gates and modules separately using Custom Designer Schematic Editor jointly with Hspice. This is to visually assemble the circuit schematic and simulation works are done to verify the gates. Output waveform can be viewed in WaveView. After a correct result is obtained, a symbol is created for the particular schematics and it is combined with other circuits to form a complete 4x4 bit multiplier using Vedic mathematic approach.

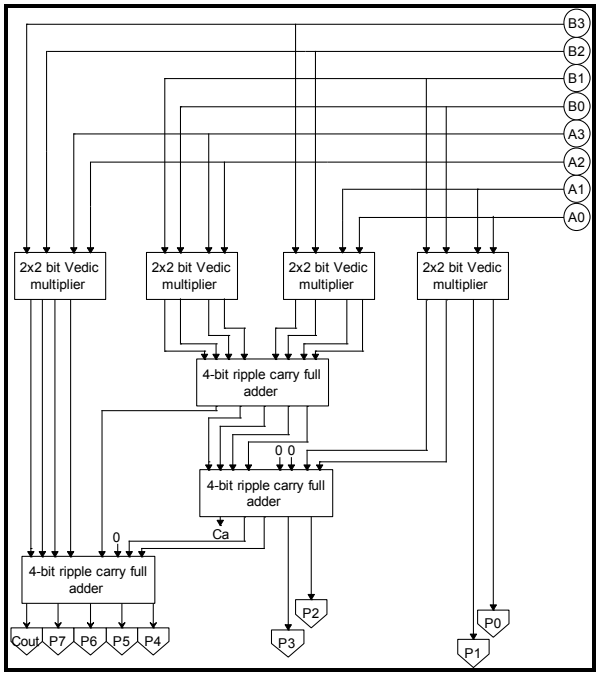

Figure 2 Block Diagram for 4x4 bit Vedic Multiplier

4. Comparison of Different Voltage Supply used in 4x4 Bit Vedic Multiplier

Using four different voltage supplies as stated, the 4x4 bit Vedic multiplier is simulated and the circuits are being compared in terms of output waveform, power consumption, and delay. For comparison in a common environment, the 4x4 bit Vedic multiplier had been simulated using the same circuit and common test bench for all voltage supply stages. Table 2 shows the result of the simulation.

Table 2 Comparison of Different Voltage Supply for 4x4 Bit Vedic Multiplier

Voltage Supply (V)	Power Consumption (W)	Delay (s)
0.9	31.48 µ	32.7 p
1.0	0.215 m	376 p
1.2	0.297 m	31.6 µ
1.5	1.171 m	52.8 µ

Based on the result obtained, the 4x4 bit Vedic multiplier with the voltage supply of 0.9 V consumed the least power consumption and produced the shortest delay among all. However, the main drawback for the multiplier using 0.9 V is the multiplier fail to produce output with a full swing waveform. The output waveform for logic '1' produced by this circuit is only able to achieve 20% of the full swing voltage. Furthermore the voltage supply of 0.9 V is not suitable for this multiplier because it will suffer when cascaded to form higher bit multiplier and this will affect the accuracy of the output result.

As for the 4x4 bit Vedic multipliers with the voltage supplies of 1.0 V, 1.2 V and 1.5 V, all the circuits are able to produce output achieving 80-100% of the full logic level. However when compared in term of power consumption, the multiplier with voltage supply of 1.0 V only used 0.215 mW which is 27.61% and 81.64% less than the circuits with the voltage supply of 1.2 V and 1.5V respectively. Besides, the multiplier with 1 V voltage supply also produced the least delay among the three voltage supplies. The output waveform of 4x4 bit Vedic multiplier with 1 V voltage supplied is shown in *Figure 3*.

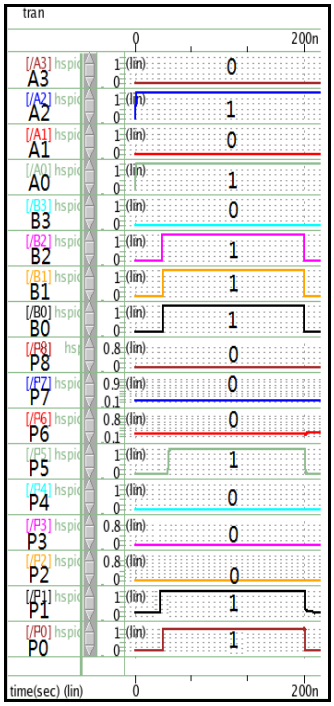

Figure 3 Output Waveform for 4x4 bit Vedic Multiplier

5. Conclusion

In this paper, a 4x4 bit Vedic multiplier has been simulated using different voltage supplies. The design was simulated using Synopsys Custom Tools in General Purpose Design Kit (GPDK) 90 nm CMOS technology process. The 4x4 bit Vedic multiplier with voltage supply of 1 V has the merits of least delay (376 ps), lowest power consumption (0.215 mW) and produced output voltage with a full logic level. Thus the combination of Urdhva Triyakbyam Sutra and 13T hybrid full adder which had been used in this project to form a 4x4 bit Vedic multiplier can be considered a good circuit with a low power consumption and delay.

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