Optimum Phase Selection of Multiphase Interleaved DC-DC Boost Converter for Current Stress and Switching Devices Losses Reduction

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Abstract: This paper presents the optimization of 2-phase interleaved DC-DC boost converter (IBC) in order to achieve switching device losses and current stress reduction. Principally, the distributed of input currents in 2-phase IBC can reduce the current stress on components i.e., inductor and switching devices, consequently the lower rating of inductor and switching device can be considered. However, the interleaving technique does not reduces the inductor current ripple in 2-phase IBC. The comparison of switching device losses and the current stress for conventional DC-DC boost converter (1-phase IBC), 2-phase IBC, and 3-phase IBCs are provided in this paper. The 180-degree phase-shifted pulse width modulation technique (PWM) is implemented on the 2-phase IBC. The results show that by increasing the phase number of IBCs, 1-phase, 2-phase and 3-phase, the switching device losses are reduced i.e., 76 mW, 30 mW, and 22 mW, respectively. Meanwhile, the inductor current stresses is reduced as well, i.e., 0.8 A, 0.4 A, and 0.27 A, respectively. The finding shows the conduction loss decreases when the phase number of IBC increases. However, this will increases the switching loss of the IBC. Thus, the 2-phase IBC is selected as the optimum phase of IBC with regards to the switching loss and conduction loss consideration of the semiconductor devices.

Keywords: Multiphase IBC, interleaving technique, current stress, current ripple, semiconductor loss, conduction loss

1. Introduction

Generally, power converters such as DC-DC boost converter are required in order to provide high DC voltage for several applications such as electric vehicle (EV) systems, photovoltaic (PV) systems, and fuel-cell system [1]–[4]. DC-DC converter is one of the power converters that is designed to process the energy deliver to the load. Normally, conventional DC-DC boost converter suffered high switching device losses and consequently will reduce the converter efficiency due to the limitation of circuit structure. Thus, in order to reduce the switching device losses, i.e., switching loss and conduction loss, an interleaving technique with multiphase circuit is introduced to achieve the reduction of inductor current ripple and current stress [5], [6]. Multiphase is defined as parallel branches of circuit, while interleaved can be defined as all branches are working in phase-shifted to each other by considering similar switching frequency and duty cycle [5]–[7]. According to the [5], [6], [8], [9], the main advantage of the multiphase IBC over the conventional DC-DC boost converter is it can solve the issues of current stress and inductor current ripple. As mentioned in [10], when high current and low voltage at source are considered, a multiphase with an interleaving technique is considered to reduce the inductor current ripple as well as current stress. By considering the improvement

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of circuit structure, the input current is evenly distributed to each branch of the multiphase circuit branches which the reliability of circuit is improved to be more efficient. Theoretically, the reduction of conduction loss can be achieved due to an even current sharing and current stress between phases at the input side. Besides, the multiphase IBC is an attractive option for high power and high current applications with low current ripple [11]. The 2-phase IBC has shown the optimum phase for switching device losses and current stress reductions at the components by considering the specifications in this paper. Thus, the performance of the 2-phase IBC is observed for switching device losses and current stress reductions. The comparison of conventional DC-DC boost converter and 3-phase IBC also provided in this paper.

2. Principle of Conventional and 2-phase Interleaved DC-DC Boost Converters

Basically, the conventional DC-DC boost converter consists of one diode (D), one switch (S), an input inductor (L) and a capacitor (C) at the output side, Fig. 1. Meanwhile, in 2-phase IBC circuit structure consist of two diodes, two switches, two input inductors, and a capacitor, Fig. 2. Generally, the circuit structure of conventional DC-DC boost converter suffered high switching device losses due to the limitation of circuit structure, Fig. 1. Practically, high current stress at the input side caused the selection rating of inductor is high and costly. However, the unique feature of 2-level IBC circuit structure able to reduce the current stress at the inductor and switching devices, consequently low rating of inductor can be selected and switching device losses reduction can be achieved.
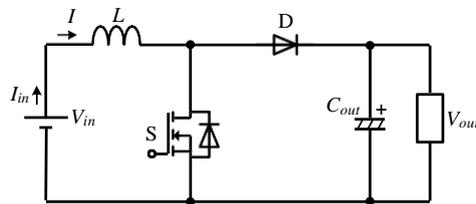

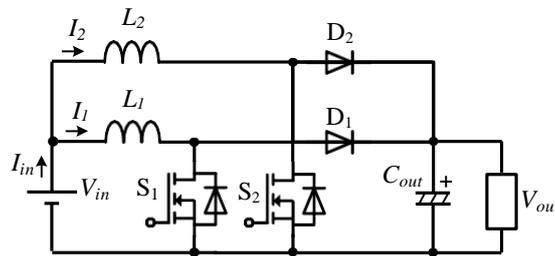**Fig. 1 - Conventional DC-DC boost converter**

Fig. 2 - 2-phase interleaved DC-DC boost converter (IBC)

Fig. 3 shows the operation modes of 2-phase IBC that operates in interleaving operation. Fig. 4 shows 180 degree of phase shifted pulse width modulation (PWM) for the switching device in 2-level IBC. The operation shows the phases operate in interleaved where the phase delay is shifted after another. The phase-shifted for each phase is expressed as follows,
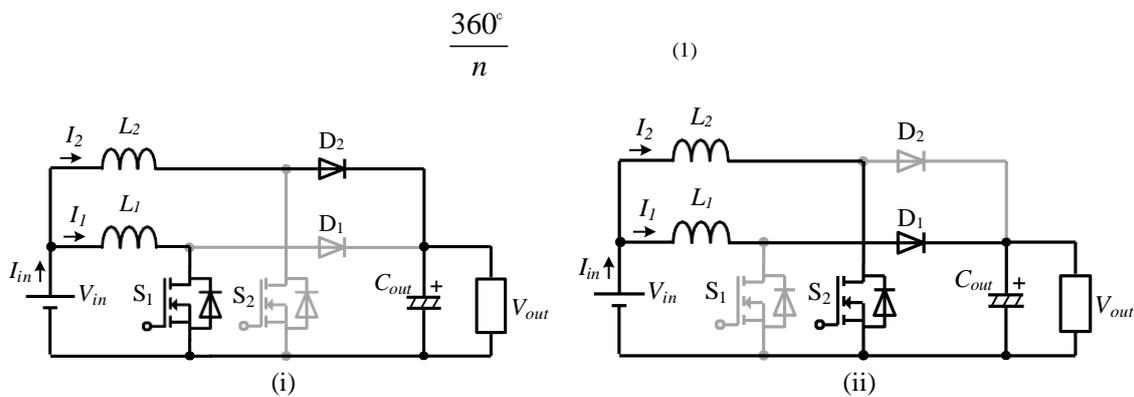
$$\frac{360°}{n} \tag{1}$$

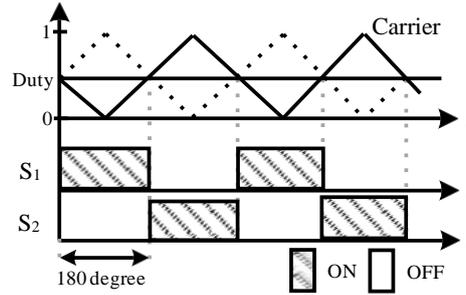**Fig. 3 – Operation mode of 2-phase IBC (i) Mode 1 (ii) Mode 2**

Fig. 4 - 180-degree phase shifted PWM of 2-phase IBC

3. Parameters Design of Conventional and 2-phase Interleaved DC-DC Boost Converters

Tables 1 shows the specification of conventional DC-DC boost converter and 2-level IBC are considered in this paper. Principally, the inductor current ripple is considered in order to design inductor. Basically, the continuous conduction mode is considered in this paper. In DC-DC boost converter design, continuous conduction mode is the most preferred operation mode for high power application over the discontinuous conduction mode. This is because the continuous conduction mode has an advantage of lower conduction loss and smaller current stress on the semiconductor devices [12]. Thus, the minimum inductance for the converter circuit in continuous conduction mode and the output capacitance of the converter can be expressed as follow,

$$L_{\min} = \frac{D(1-D)^2 R}{2 f_{sw}} \qquad (2)$$

$$C_{out} = \frac{D}{R f_{sw} r} \qquad (3)$$

where R is the resistance, f_{sw} is the switching frequency, r is the voltage ripple factor. The output voltages of the converters are controlled independently by varying the duty cycle D. Meanwhile, the output voltage V_{out} and boost ratio β of the conventional DC-DC boost converter and 2-phase IBC can be expressed as follow,

$$V_{out} = \frac{1}{1-D} V_{in} \qquad (4)$$

$$\beta = \frac{1}{1-D} = \frac{V_{out}}{V_{in}} \qquad (5)$$

3.1 Current Stress and Input Current Ripple Reductions

Input current ripple is occurred due to the switch are turn-ON and turn-OFF which produce ripple. The input current ripple must be considered according to the application which required small current ripple at the input side. Usually, the input current ripple reduction can be achieved by considering a large input inductor. However, this will increases the size and weight of the converter [13]. Thereby, an interleaving technique is considered where the input current ripple reduction can be achieved by summation of all phases of current ripples. Fig. 5 shows the principle of input current ripple reduction when interleaving technique is applied. By increasing the phase number of IBC, input current ripple is reduced significantly. Fig. 6 shows the current stress of each phase is reduced with similar inductor current ripple when the phase number of IBC is increased. Thus, this condition can easily be written as follows:

$$\Delta I_{in(3\text{-}phase)} < \Delta I_{in(2\text{-}phase)} < \Delta I_{in(conv)} \qquad (6)$$

$$I_{L1(3\text{-}phase)} < I_{L1(2\text{-}phase)} < I_{L(conv)} \qquad (7)$$

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$$\Delta I_{L1(3\text{-}phase)} = \Delta I_{L1(2\text{-}phase)} = \Delta I_{L(conv)} \qquad (8)$$
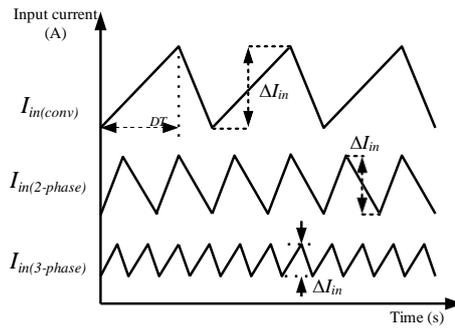

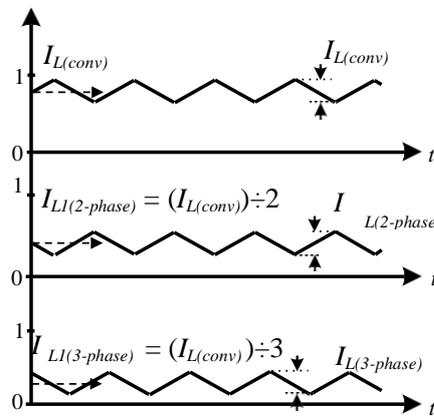**Fig. 5 - Input current ripple reduction of multiphase IBC**

**Fig. 6 - Reduction of current stress in conventional DC-DC boost converter,
2-phase IBC and 3-phase IBC**

3.2 Switching Device Losses Reduction

There are mainly two kinds of losses that occurred in switching devices which are conduction loss and switching loss [14]. Generally, the conduction loss and the switching loss of MOSFET are expressed as follow, respectively,

$$P_{cond(m)} = I_{ds}^{2} \times R_{on} \times D \qquad (9)$$

$$P_{sw(m)} = \left\lceil \frac{(I_{ds} V_{ds}) \times (t_r + t_f)}{6} \right\rfloor (f_{sw}) \qquad (10)$$

Conduction loss P_{cond} is proportionally to the squared of drain-source current I_{ds}. Thus, the conduction loss is significantly decreased when drain-source current is decreased. These can be achieved when interleaving technique is applied by increasing the phase number. Meanwhile, the diode only consists of conduction loss $P_{cond(d)}$ which depends on forward rms current $I_{f(rms)}$ where it considers the maximum and minimum current of diode.

$$P_{cond(d)} = I_{f_{(rms)}} \times V_f \times (1 - D) \qquad (11)$$

However, this paper only considered MOSFET conduction loss in the analyses. Fig. 7 shows the relationship between conduction loss and switching loss against the phase number of IBC. It shows that the conduction loss is decreases when the phase number of IBC is increased. Meanwhile, the switching loss is increases as the phase number

of IBC increasing. Thus, an optimum phase of IBC must be considered in order to achieve high efficiency of converter. From the illustrations, the optimum phase number of IBC is occurred when the conduction loss and switching loss is across each other. Besides, it depends on the output power of converter.
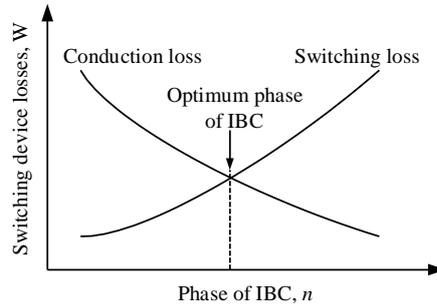
Fig. 7 - Losses against phase number of IBC

4. Results and Analysis

The specifications of the simulation and experimental works is shown in Table 1. The MOSFET considered in the experimental is SPW21N50C3

**Table 1 - Specifications of conventional DC-DC boost converter and 2-phase IBC**

Parameters	Value
Output voltage, V_{out} (V)	60
Switching frequency, f_{sw} (kHz)	200
Duty cycle, D	0.5
Voltage ripple factor, r (%)	1
Resistor, R (Ω)	150
Inductor, $L_{conv} = L_{(2-phase)}$ (mH)	1
Output capacitor, C_{out} (μF)	1200
Output power, P_{out} (W)	24

4.1 Current Stress Reduction

By considering interleaving technique, the current stress reduction on inductor is achieved. The current stress of conventional DC-DC boost converter, the 2-phase IBC, and the 3-phase IBC are observed. Fig. 8 shows the simulation results of the inductor current stresses on conventional DC-DC boost converter, 2-level IBC and 3-level IBC, respectively. Meanwhile, Fig. 9 shows the simulation results where the current stresses reduction is achieved at MOSFET of the 2-phase IBC and 3-phase IBC.
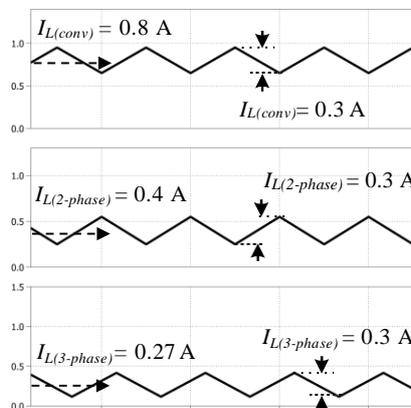

**Fig. 8 - Simulation result of current stress on inductor**
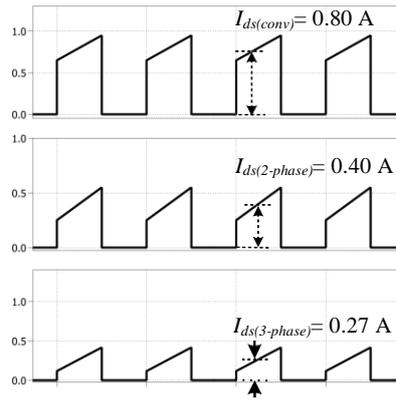
**Fig. 9 - Simulation result of current stress on switching device (MOSFET)**

The principle of DC-DC boost converter is to boost-up from low input voltage to high output voltage. The output voltage is boost-up depending on the duty cycle D. For the experimental specifications, the selected input voltage is 30 V and the output voltage is then boost-up to 60 V with 50% of duty cycle. Figs.10, 11 and 12 show the current stress on inductor for the conventional, the 2-phase IBC and the 3-phase IBC. It is experimentally confirmed that the inductor current stress for each phase is decreased when the phase number of IBC is increased.
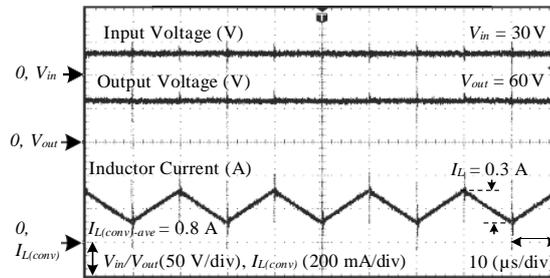
Fig. 10 - Input voltage, output voltage and inductor current stress/ripple of the conventional DC-DC boost converter
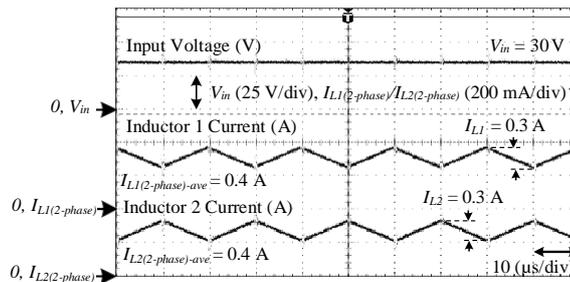
Fig. 11 - Input voltage and the current stress/ripple of the 2-phase IBC
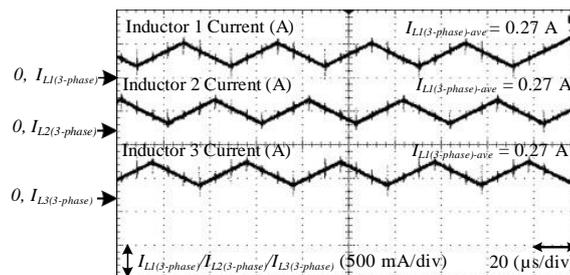
Fig. 12 - The current stress/ripple of the 3-phase IBC

4.2 Input Current Ripple and Current Reduction

Conduction loss occurred when there is conduction current or energy dissipated by components in a circuit while MOSFET is turn-ON. As discussed at previous sections, the conduction loss is decreased as the phase number of IBC is increasing. Meanwhile, switching loss occurred during transition of turn-ON and turn-OFF for some periods of time. Thus, the switching loss will be increased as the phase number of IBC increases where proportionally to the number of switching devices used. Several data are recorded in analyzing the losses occurred in switching devices. Tables 2 and 3 show the switching loss of MOSFET during turn-ON, $P_{sw(on)}$ and turn-OFF, $P_{sw(off)}$. Meanwhile, Table 4 shows the conduction loss in MOSFET and Table 5 shows the total losses of MOSFETs for the conventional DC-DC boost converter, 2-phase IBC and 3-phase IBC. Meanwhile, Fig. 13 shows the relationship between switching device losses and phase number of IBC based on the analyses in this study. It can be observed that the 2-phase IBC has the optimum of switching loss and conduction loss as compared to the 1-phase conventional boost converter and the 3-phase IBC based on the switching device losses characteristic as shown in Fig 7. Thus, the optimum phase of IBC with the load considered in this paper is 2-phase IBC.

Table 2 - Dissipated energy during turn-ON

Phase of IBC Parameters	1-phase Conv.	2-phase IBC	3-phase IBC
I_{ds} (A)	0.65	0.25	0.12
V_{ds} (V)	60	60	60
t_r (ns)	5	5	5
$P_{sw(on)}$ (mW)	8	8	8.1

Table 3 - Dissipated energy during turn-OFF

Phase of IBC Parameters	1-phase Conv.	2-phase IBC	3-phase IBC
I_{ds} (A)	0.95	0.55	0.42
V_{ds} (V)	60	60	60
t_r (ns)	4.5	4.5	4.5
$P_{sw(on)}$ (mW)	7.20	7.20	7.29

Table 4 - Conduction loss in MOSFET

Phase of IBC Phase of IBC	I_{ds} (A)	$R_{ds(on)}$ (Ω)	D	P_{cond} (W)
1-phase Conv.	0.8	0.19	0.5	0.061
2-phase IBC	0.4	0.19	0.5	0.015
3-phase IBC	0.27	0.19	0.5	0.007

Table 5 - Switching devices losses

Phase of IBC Phase of IBC	P_{sw} (mW)	P_{cond} (mW)	P_{mosfet} (mW)
1-phase Conv.	15	61	76
2-phase IBC	15	15	30
3-phase IBC	15	7	22
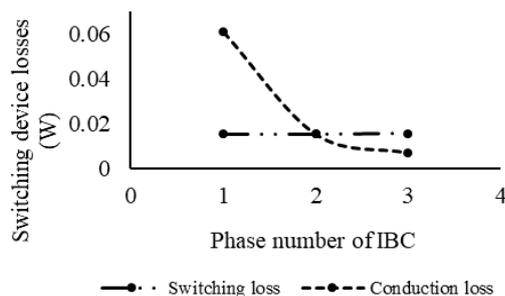
Fig. 13 - Switching device losses in MOSFET against phase number of IBC

5. Conclusion

In this paper, it is concluded that the switching device losses and current stress at the components are able to be reduced with considered 2-phase IBC by implementing the multiphase circuit structure and interleaved technique. Due to the unique features of the multiphase IBC circuit structure, it reduces the selection rating of the components, conduction loss and the failure rate of the converter. However, the additional of switching devices cause the switching loss increases. Thus, by concerning in this issue, the optimum phase of IBC must be considered in order to obtain the lowest of the switching and conduction losses. By referring the semiconductor losses, the optimum phase of IBC is 2-phase as discussed at the Section 4.2. The volume and size reduction of the inductor in the 2-phase IBC can be considered in the future due to the unique feature of the circuit structure.

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