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Quantum-dot Cellular Automata: Review Paper

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Abstract: Quantum-dot Cellular Automata (QCA) is one of the important discoveries that is designed to be a successful alternative for CMOS technology in the near future. An important feature of this technique, which has attracted the attention of many researchers, is that it is characterized by its low energy consumption, high speed, and small size compared with CMOS. Inverter and majority gate are the basic building blocks for QCA circuits, where it can design most logical circuits using these gates with help of QCA binary wire. Due to the lack of availability of review papers, this paper will be a destination for many researchers interested in the QCA field, how it works, and why it's taking lots of attention recently.

Keywords: Quantum-dot Cellular Automata, QCA, Nanotechnology

1 Introduction

In order to overcome the physical limitations of Integrated Circuits (IC) created by CMOS technology, which is created using expensive lithography, short channel effects, and doping fluctuation, and to make Moore's law for integrated devices valid, attention has been paid to modern nanotechnologies. One of those techniques that drew attention is Quantum-dot Cellular Automata (QCA). This promising technology supports the construction of digital circuits with unique advantages in terms of low power consumption, high speed, and high density as well. Until recently, QCA technology faced a range of challenges in order to be practical and utilizable for constructing digital circuits in a very large scale. Some of these challenges are the manufacturing process, manufacturing standards, and different design methodologies. QCA has a good chance to become the new digital system in near future [1]. This paper will try to summarize the important milestones towards making QCA technology the new technology of digital systems fabrications. Also, an attempt to highlight the aspects that are neglected and not discussed with QCA technology literature will be given in the final conclusions of this paper. The rest of this paper is arranged as follows:

Section 2 provides a background for the QCA technology. QCA modelling is highlighted in section 3. The physical implementation techniques are discussed in section 4. Power dissipation in QCA circuits is summarised in section 5 while the circuit fault tolerant detailed in section 6 in addition QCA digital design is demonstrated in section 7. Finally, this paper will conclude in Section 8.

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2 Background

2.1 Basic

QCA was introduced first time in 1993 by Lent et al [2]. The main element in QCA is a square cell containing four dots and two electrons. Columbic interaction cause electrons to occupy the dots in antipodal sides [3]. For binary computation, CMOS uses voltage levels whereas QCA uses the location of electrons inside cell. Cell polarization used to represent logic "0" or logic "1" where QCA cell will take a specific polarization depending on the electron's configurations. Switching states are carried out by allowing the particles (electrons) to tunnel between the dots mechanically. The tunnel junction is illustrated in Figure 1(a). The two types of QCA cells is shown in Figure 1(b). Due to columbic interaction, the information will exchange with the adjacent cells. Input cell will drive the neighbouring cell to be in the same polarization. So, forces the input cell to a specific polarization that's only required. Figure 1(c) shows the propagate information of neighbouring cells across a wire [4].

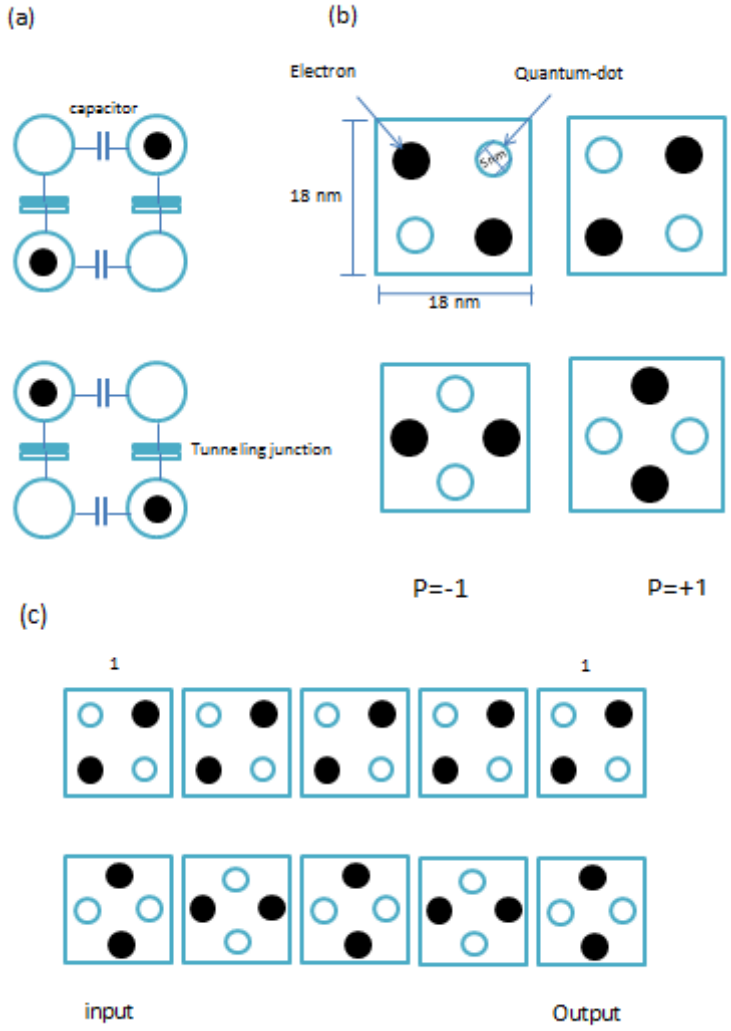

Fig. 1- QCA cells (a) Functional outline, (b) Presented forms, (c) Wire types

2.2 Clocking

Data is controlled by the clock signal and input and represented by the polarization of cells [5]. There are several reasons to make clocking very essential to QCA circuits [6]:

1- Control the flow of information: The direction of information flow from the input to the output cell can be controlled by clock signal since there is no current flow in this nano-technique.

2- Constraining the circuit to remain in the quantum mechanical ground state, which is an essential condition to duly accomplish QCA working.

3- Timing control: For the purpose of controlling the timing of QCA circuits, the clock signal should be used as it is the only tool to do this, in addition to ensuring quick switching and quick relaxation, as the clocked cells relax faster than non-clocked.

4- Creating pipelines if multiple clock signals are utilized: To prevent the KINK state, which happens when a huge number of cells are switched together. This may lead to stumbling into the minimum local energy and the circuit will not reach the ground state. The QCA circuit is split up into multiple specific zones clocked with multiple clock signals. This handles the issue of KINK state and gives pipelining for QCA systems.

5- To revive the lost signal energy to the environment: for one clock cycle the net energy in the QCA system could be expressed as:

$$E_{net} = E_i + E_{clock} - E_{diss} - E_o \quad \ldots (1)$$

Where E_{net} is the net energy change, E_i is the energy of driver (input cell), E_o is the consumed energy by the output cell, E_{clock} is the dissipated energy along the signal path. So E_{diss} is essential to compensate for the energy loss in the path to ensure a net energy change of zero.

Generally, the clock in QCA circuit has four states to ensure adiabatic switching state and to avoid abrupt switching. This happen because the input in abrupt switching changed suddenly and the circuit still in excited state, in this situation the circuit will enforced to dissipated energy to the environment to be in relax state. Therefore, the relaxation state will be uncontrollable. While in adiabatic switching, the relaxation is manipulated by both the switch phase and release phase and it accomplished by reducing the dots barrier, remove the past input, applying the present input, and after that raising the barriers of dots. If these states occur sequentially, the system will stay close to the ground state [5].

There are two commonly used types of clocking signals in the QCA circuits; the first one is Landauer [2] as shown in Figure 2, the second type is Bennett clock [7] as shown in Figure 3, which supports reversible operation and minimize the power dissipated by deleting information, but the system speed is to be impacted negatively.

The clock signals in QCA are generated by an electric field, supplied by either Carbon Nanotubes (CNTs) or CMOS burned below QCA circuit, applied to cells either to raise tunnelling barrier or to lower it. When the tunnelling barriers are low, the cells are unpolarized otherwise it becomes polarized and cannot change its state.

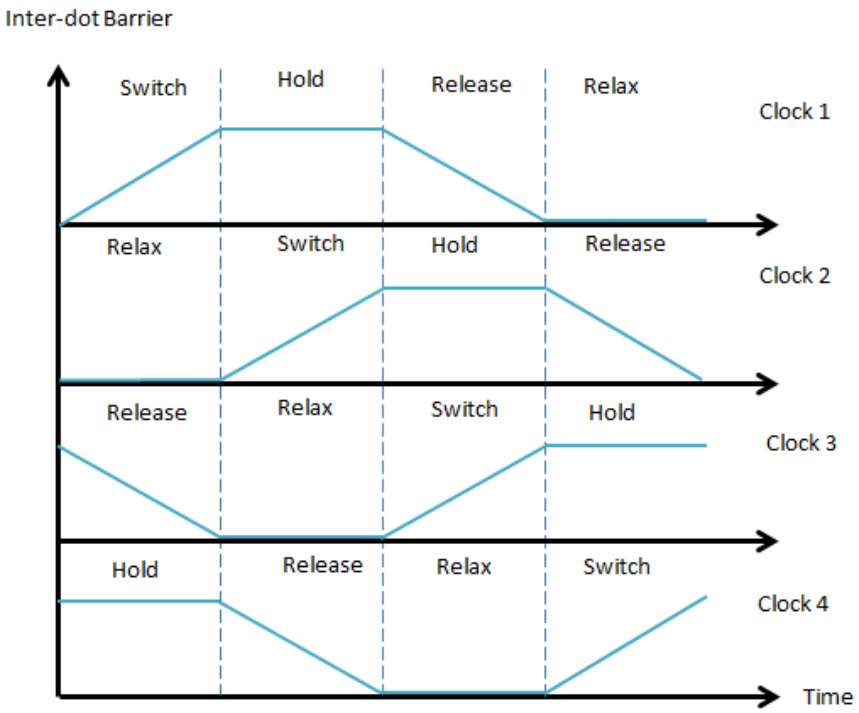

Fig. 2 - Landauer clock waveform [2]

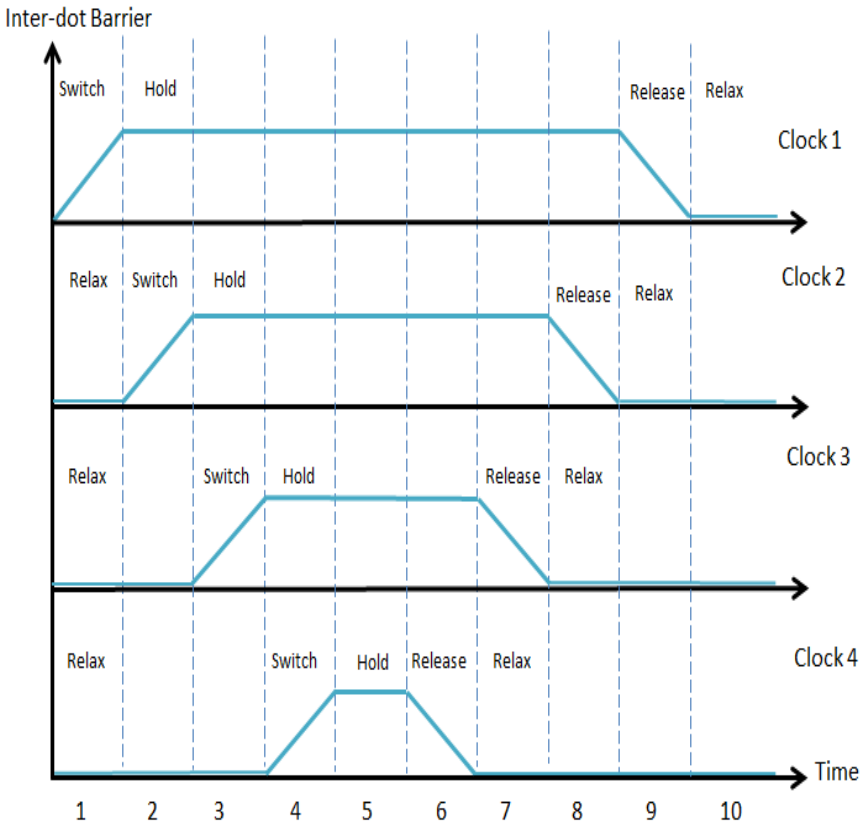

Fig. 3 - Bennett clock waveform [7]

2.3 Wire crossing

The problem of component interconnection or wire crossing in QCA technology must be solved so as to go ahead to be the good replacement for the current IC in fabrication. There are three strategies were proposed up to know to handle wire crossing in QCA [8] which are:

1- Coplanar crossing: This strategy accomplished using two types of QCA cells, these two types of wires are perpendicular to each other. One of these wires has cells in the rotating form, which means that the other wire uses non-rotating or direct cells, so it can work independently of each other and can cross in the same layer as illustrated in Figure 4(a), this type of crossing can be easily affected by manufacturing defects, which is the biggest drawback for this type. Therefore, if any cell deviates (misaligned) from its position, it will result in a cross-coupling between the operation of two wires. To increase the robustness of this type of wire crossing, many research has been done such as in [9, 10] but this leads to a significant increase in overhead.

2- Multi-layer wire crossing: This strategy needs to implement multiple active QCA layers on the top of each other which make it difficult for implementation. The crossing will be done in this method in another layer as shown in Figure 4(b), the same cell types can be used as long as the vertical distance between wires is sufficient to prevent signals leaking from one layer to another and there is a way to create cells stacked between layers.

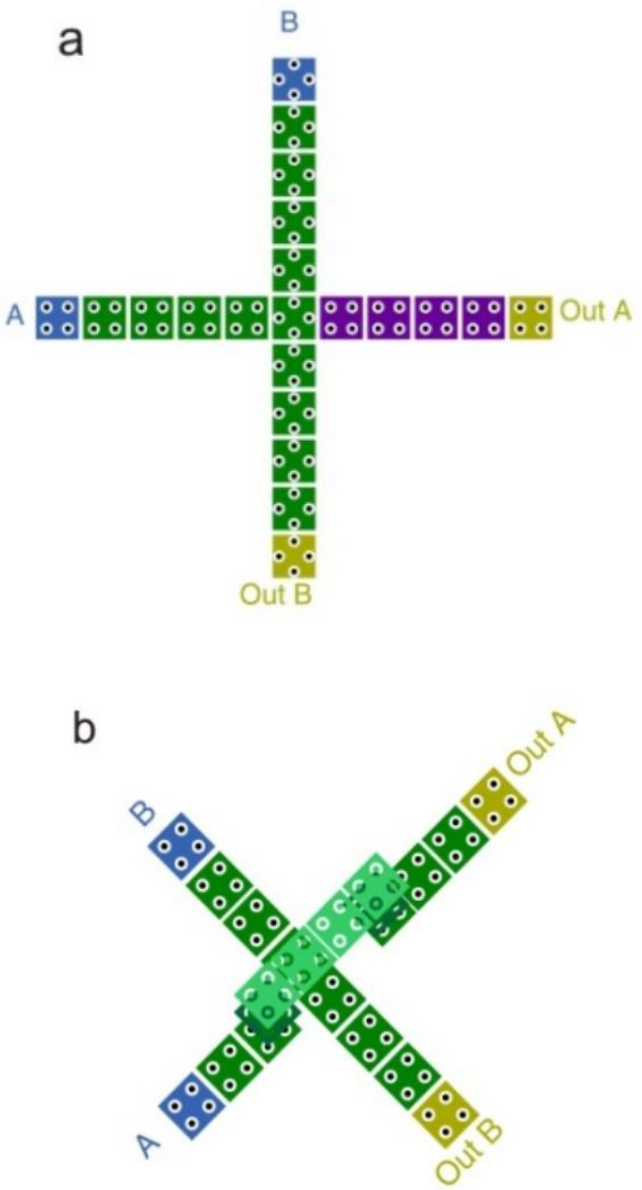

Fig. 4 - Wire crossing (a) coplanar (b) multi-layer

3- Logical wire crossing: Many methods were presented to replace physical wire crossing by a logic gate for example clock manipulation [11] and node duplication [12] or using routing algorithm for FPGA [13]. All these methods give the robustness of the circuit but it will cause a loss in speed and area. Coplanar wire crossing strategy in view of clocking phase interference and impact on each other was exhibited in [4] which is introduced simultaneously with S.-H. Shin et al [14]. Where they benefited from the fact that the cells in the release and relaxation phase have no effect on adjacent cells and they are un-polarized. Their work was summarized as follows:

Cells in Hold phase can cross cells in relax phase and cells in the switch phase can cross cells in release phase without effect on polarization as shown in Figure 5. [4].

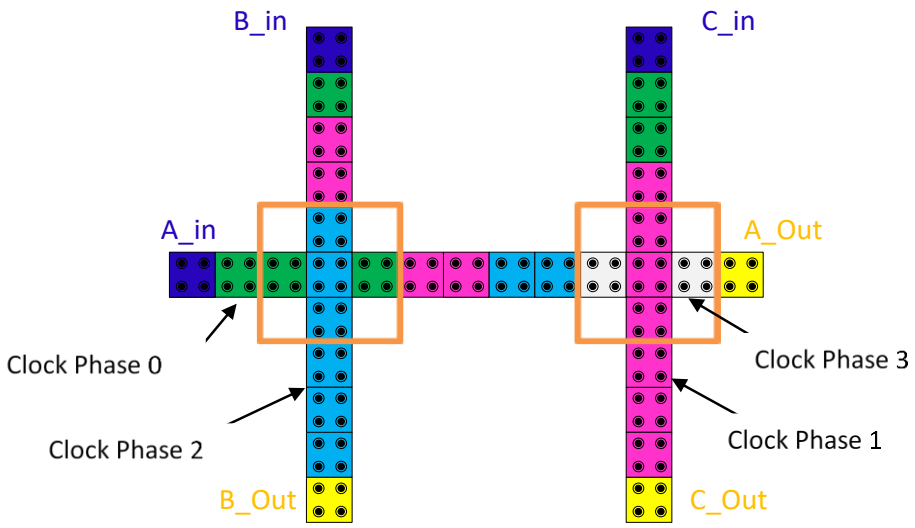

Fig. 5 - Logical wire crossing [5]

2.4 QCA Primitive Gates

In QCA, the primary logic device is the majority gate which is illustrated in Figure 6. Consequently, this gate with inverter (Figure 7) are able to form most logical gates [15].

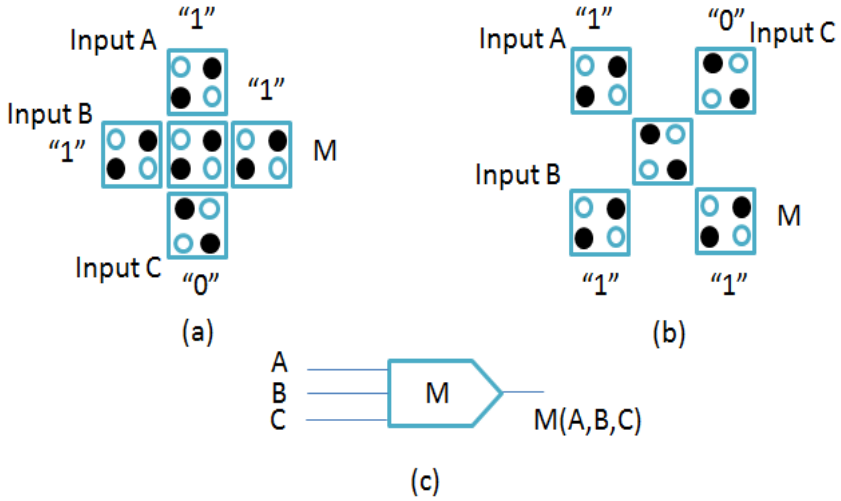

Fig. 6 - QCA 3-input majority gate (a) Ordinary form (b) Rotated form (c) Symbol [16]

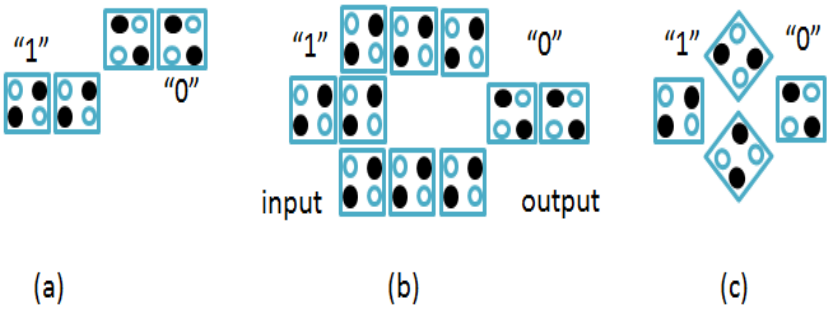

Fig. 7 - Types of logic inverters in QCA, (a) Corner approach (b) Robust design (c) Rotation [16]

In general, the simple majority gate contains three cells for input, one cell for output and a single cell in centre as a voter cell. If two or three input values set to "high", the output value will go "high", otherwise output will be "low". The typical 3-input majority gate equation is given by formula (2).

$$M(A,B,C) = AB + BC + AC \quad \ldots (2)$$

By setting the polarization of one input to the logic of "1" or "0", we can obtain the OR gate or the AND gate respectively. From these AND and OR gates, complex logic circuits can be implemented. The importance of 3-input majority gate in QCA circuits leads the researchers to think for designing multi-input majority gate such as [17, 18].

On the other hand, more than one type of the logical inverter in QCA are introduced, as in Figure 7. According to the general rule in the inverter gate, after applying a random value to the input cell, an inverted value will be produced in the output cell.

3 Modelling

A lot of models were proposed for QCA dynamic modelling and several approximations were made to produce an effective circuit simulation tool in this technique. A quantum mechanics completed model was presented in [19]. While the most important steps were presented in the approximation to find a practical model from the computation point of view and led to a simulation tool in [20-22] where Q-BART and M-AQUINAS were presented as a simulation tool for QCA large circuits. Other attempted to create a SPICE model for Metal-dot QCA [23]. QCADesigner was introduced in [24] which is the most common design tool for simulation QCA circuits. The drawback of this software and others is their inability to deal with multi-type clocking signal. All of them use the Landauer clocking type. Verilog HDL to develop the QCA library introduced in [25] but this library has a drawback where it does not include the dynamic behaviour of the cell because Verilog is unable to handle QCA dynamic equations [6], therefore this library could not be applied for practical QCA modelling. So a library for the components of QCA utilizing VHDL-AMS on the behavioural level exhibited in [26] where the primary QCA blocks were described. In this library, the clock was defined as a state variable with four states and the timing for the transition between states can be controlled with the clock cycle.

Abstraction scale can be raised so as to cope with the complexity of the large system and to develop a flow of systematic design, but this critical area has been only previously studied for QCA. A methodology by detail was described using modelling with VHDL language in [27]. The tile-based approach was presented in [28-32] and the systematic structure of sequential systems in [33-35]. Locally Synchronous Globally Asynchronous (LSGA) design approach was adjusted for QCA to accomplish layout timing autonomous operation in [36-38].

To find a precise model of the QCA cell, many bodies Schrodinger equations are needed, but this will result in a model that is applicable only to pairs of cells where the burden of computation accumulates exponentially with the number of cells, so this model cannot be used to verify the system [39] by assuming the cells as a system with two states, an approximation can be made so as to increase the size of the circuit to 10-15 cells. The Hartree-Fock is the method which capable of producing a practical tool for simulate large QCA circuit. This method can model the intercellular interactions with classical Columbic coupling and intercellular dynamics quantum mechanically [19]. This approximation was used by the QCADesigner for both simulation engines (coherence and Bistable) [24].

4 QCA physical implementation Techniques

For building a QCA cell physically, different ways were introduced with bi-stability and controlling the local interaction and applying clock, but the material systems are at the beginning of their evolution. A large number of researches have focused on the columbic interaction between cells for performance improvement, implemented with metal-dot, semiconductors or molecular approaches [6, 40]. A prologue to early work on the difficulties of QCA execution can be obtained in [41]. Enhancing the cell level to achieve the robust ground state is in [42, 43], and following genuine 3-dimensional techniques to expel metastable states suggested in [44]. Proposition of the concept of restricted minima quantum-dot arrays (RMQDA) based on non-clocked (passive) wires and active clocked amplifier segments introduced in [45], a proposed technique based on resonant tunnelling currents such as split current QCA (SCQCA) is found in [46]. The main approaches to the physical QCA implementation are summarized below, as the first three are based on the electrostatic interaction while the fourth is based on the magnetic interaction [39].

Metal-Island QCA: The manufacturing based on the effect of the Coulomb blockade in tunnel junction linked with metallic islands has been explained in the laboratory environment, but because the size of the feature is quite large (the distance dot-to-dot is around one-micron), quantum mechanics required for operation exist only in cryogenic sub-Kelvin temperatures. Experiments were conducted typically at 15 mK [47], utilizing liquid helium cooling, whereas 300 mK has been the highest temperature achieved. This approach allowed small circuits to demonstrate the concept (low-temperature

prototypes of the future molecular systems). It has been shown that the bi-stable cellular automata can be switched and realized by electrons tunnel control, but it is not practical to construct large circuits in this way.

Molecular QCA: It is considered one of the most popular solutions proposed in terms of QCA physical implementation, and it depends on individual molecules acting as cells. The smallest and most performing QCA cell can be performed with a molecular system. Because many molecules are in nanoscale, the device's density for the chip can increase significantly, leading to highly complex digital systems. In addition, theoretical frequencies are estimated up to THz, still assuming operating temperature at a non-cryogenic [39, 48]

Semiconductor QCA: The implementation of semiconductors for electrostatic cells ensures a comprehensive manufacturing process for QCA circuits, as the industry now has many years of experience in continuous improvement of processes. The biggest challenge here is to achieve a very small feature size so that the circuits operate at temperatures over the sub-Kelvin. The future lithography process may be small enough to enable a somewhat higher temperature, up to about 77 Kelvin, which can be acceptable in a supercomputer. The imaginable application is the traditional part of the quantum computer, with the modern cooling system [39].

Magnetic QCA: Another kind of QCA which stores data utilizing bistable magnetic cells and moves data between cells by utilizing the magnetic coupling. The advantages of this type are relatively large feature sizes and the availability of additional quantum effects at high temperatures, which in turn simplifies the process of manufacturing. There have been some suggestions for the implementation of magnetic QCA, but it is common for all of them to have restricted operating speed, for nano-magnets ranging from 10 to 100 MHz [39].

5 Power Dissipation

power dissipation is a very important issue in all electronic devices, and because QCA is a new technology for design electronic circuits so it's very important to study the above feature in order to get minimum power dissipation. Dissipated power in QCA designs was calculated by [49, 50] and several attempts to design QCA based gates and circuits with minimum power consumption such as [3, 51-57]. Thermodynamic analysis for reversible computing designed by QCA technology in [58], a mechanical model of energy in QCA [59], dissipated power in the clocking wires was analysed by [60]. In 2011, a new tool (QCAPro) was presented by S. Srivastava et al [61], this most common tool used to estimate the switching power loss in QCA and polarization error. Data flow algorithm in QCA circuits was proposed in [62], this algorithm used to evaluate complex QCA designs and relies on the potential energy of QCA cell dots. Comprehensive analysis of power dissipation in QCA was introduced in [63].

The analysis of power consumption in QCA is very important since this technology has no current flow, so inspecting other causes for power dissipation can decrease the overall power consumption of the circuits.

6 Fault Tolerant, Defect and Testing

The basic QCA defects types (missing, displacement, and misaligned) were described and a testing diagram was proposed in [64-72], the effects of cells size scaling were investigated in [73, 74], characteristics analysis of defect tolerance in tile-based design in [30, 31] and sequential system in [33-35]. The consequences of timing errors and clock shifts were simulated at [75-78], tolerance of general displacement in [79-81]. The probability of fault switching specified by utilizing probabilistic networks in [82], thermal robustness schemes of wire crossing in [9, 10], the fault masking was taken at the logic level in a crossbar-based programmable logic array (PLA) in [83] and the possibility of applying the N-detect test in error testing to QCA designs in [84]. The faults in one-dimensional logically reversible QCA arrays were studied in [85-87] using the vital nature of gates to greatly simplify testing. Test pattern generation was developed for synthesis QCA logic in [88-90]. To detect run-time errors in the system, support for totally self-checking (TSC) tuning tool in threshold logic circuits was introduced in [91]. Block gates were presented for fault tolerance in [92-94] and triple modular redundancy with shifted operands as a fault tolerant technique was proposed to improve circuit in [95].

On the other hand, some paper discussed the reliability of QCA circuit [93, 96, 97], most of them used method called Probabilistic Transfer Matrix (PTM).

All the aspects discussed above are still speculations of the defects and faults and highlighted expected problems. The implementation of QCA technology in commercial chips will open this research scope widely.

7 Digital Design

In addition to developing basic implementation technology, there has been worthy research in the design of circuits and systems using QCA. The goal of the early research is to shorten the time needed to master the technique, using characteristics from physical design to high-level system design; sub-gate level pipelines, coplanar wire crossing,

memory-in-motion paradigms, and processing-in-wire which enable low cost logic are new design challenges [39]. Programmable Logic nano-scale circuits and designs should endure higher rates of imperfections than the present circuits, and the required redundancy can be adaptably supplied by a programmable processing platform. A reconfigurable logic for QCA has been presented in [11, 83, 98-101].

7.1 Simple processor

Besides the basic logic, more sophisticated designs have been proposed for QCA, aimed to carry out the tasks of signal processing. Where basic arithmetic circuits for example adders and multipliers, using majority gate in 3-input and complex form, was introduced in [102-105]. Then this arithmetic circuit became faster, smaller and simple [106-108] after introducing majority gate with 5-input (Maj-5) [109]. For telecommunications issues, a serial bit-stream analyser (SBSA) was introduced in [27, 110]. For image processing, a Single Instruction Multiple Data (SIMD) arrays propagated instruction processor (PIP) in [111]. The hybrid architecture of Fast Fourier Transform (FFT) with data permutation produced utilizing QCA by [112] and basic stochastic computing blocks for signal processing in [113]. A microprocessor with a general purpose such as Simple12 was proposed in [21, 22, 77, 114-116] with universal clocking floorplan, and a design depending on accumulator architecture in [117-126]. QCA based FPGA or its building block (CLB) have been presented in [127-137].

7.2 Sequential Circuit

Many researchers focus on sequential circuit based QCA. An empirical demonstration of a clocked QCA shift register (SR) with two-stage and utilize it to simulate the operation of SR with multi-stage [138]. Analysis with detail for sequential circuits design in QCA has been done in [33], a method of falling edge triggered and provide a detailed analysis of circuits designed in QCA was proposed in [139]. QCA synchronous counters in a single layer using T flip-flop [140] and using JK flip-flop [141]. QCA dividers presented in [142]. 4-bit and 8-bit Universal shift register (USR) using new QCA D flip-flop and multiplexer were proposed in [143], new n-bit synchronous counter using new level-sensitive flip-flop introduced in [144, 145]. 4-bit synchronous counter with low cost and overcome some previous limitation introduced in [146].

Adapting the conventional logic design techniques to design sequential circuits in QCA technology needs to be avoided by researchers. The inherent capabilities of QCA technology need to be considered in future designs.

7.3 Memory Unit

There is no doubt that the memory is very important in digital systems and since the QCA system is one of the modern systems in the design of digital circuits, the researchers focus on the memories and how to implement it in the QCA. Despite the fact that QCA is innately a self-latching technology, where even basic wires work as shift registers, a few universally useful structures have been proposed to empower conventional RAM type addressable memory. The most presented designs circulate bits stored continuously inside wire loop in QCA, the value refreshing dynamically, and producing a serial memory [32, 147, 148], a completely parallel memory unit with one bit for every loop [24, 117], or hybrid parallel-serial [149, 150]. More complex memory, H-structured, and a similar implementation model were proposed in [151, 152]. In addition loop-based approach for QCA memory implementation, new approach was introduced in QCA called line-based memory [153, 154] but it required special timing and clocking zones.

A scheme to investigate the basic memory structures timing utilizing Verilog modelling has been introduced in [155]. QCA memory unit without crossover having set/reset ability was introduced in [53, 156-159] while [160] introduces same memory cell but without ability for resetting and setting. Another type of memory called Content Addressable Memory (CAM) was introduced in QCA by [161-164]. CAM is a kind of memory where the input is a data word rather than memory address as in RAM. CAM looks for the data word to verify if it is saved anywhere in it. CAM gives the position where an input word can be found. CAM is frequently utilized in network switches.

Memory circuits in both types not optimized enough [165] so attention should be paid to use the inherent capabilities of QCA circuit for building optimal memories as done before in many previous circuits such as XOR circuit [166] and multiplexer [55].

8 Conclusions

This paper presents a review for the researches that focused on the QCA technology and gives extensive detail about this new nano-technique. In addition, previously published research has been classified as a basic base for researchers wishing to expand into a specific field within this technique. QCA technology needs a lot of work to be a successful alternative to the CMOS technology. Many challenges in this field need more considerations; one important

aspect is the interface of QCA circuits with other devices and circuits, the multi-layer physical implementation also needs lighter on. QCA technology has inherent capabilities for digital circuit design without following any Boolean function. This approach is done before in literature for designing many important circuits such as XOR and MUX. Although memory circuits are very important in digital design, it is not optimized enough, so inherent capabilities can be used to build memory circuits or its building blocks.

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