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A Content-Addressable Memory Structure using Novel Majority Gate with 5-input in Quantum-dot Cellular Automata

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Abstract: Quantum-dot Cellular Automata (QCA) technology is one of the most important new nanotechnologies and is a suitable replacement for CMOS circuits. Majority gate and Inverter are the primary building blocks in QCA circuits. Content Addressable Memory (CAM) is a type of memory used in applications that require high speed. In this paper, a novel five input majority gate is introduced. This gate is simulated with QCADesigner tool and compared with previous same structures. Then, the proposed gate used to design a CAM cell in a single layer after deriving the minority gate from the proposed majority gate. The proposed CAM cell has a simple and robust structure and does not require wire crossover, also it reduces circuit complexity by 7% in term of cell count compared to existing structures.

Keywords: Quantum-dot cellular automata (QCA), Content Addressable Memory (CAM), Five input majority gate, Nanotechnology

1. Introduction

In recent years, most digital devices such as computer and media devices have been converted to portable. These devices have batteries and that is why designers tried to find new ways to reduce their consumption of power. Moreover, power consumption and speed are very significant indices for VLSI circuits performance. Recently, QCA circuit design with low-power has obtained more attention [1]. QCA is an advanced electronic nanotechnology that provides logic states, not as voltage levels but depends on the placement of electron pairs [2]. QCA depends on the mutual attraction and repulsion of electrons. The primary element in QCA is a four dots square cell and two additional electrons. Because of the Columbic interaction, these electrons settle inside the dots in a diagonal position [3]. QCA designers have spent a lot of time trying to design circuits in QCA with low complexity. In general, The core components in QCA circuit are majority gate with inverter whereas a better QCA circuit can be accomplished by optimizing this component [1].

The design of high-efficiency memory in the QCA system has caught many researchers' attention. A set of research such as [2, 4-8] focused on this issue, but these works have been implemented on the Random Access Memory (RAM) model where each location in this memory is accessed by a particular address. In this work, CAM is described, which is

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different from RAM, since in CAM the memory location is accessed by its content. CAM is a special type of memory used in high-speed applications where it is possible to significantly reduce the time spent searching for a stored item in memory if the data stored can be identified by the content rather than the addresses [3].

In this paper, a novel majority gate with five-input is firstly introduced then the minority gate is carried out. CAM cell based on the proposed minority gate was designed. Finally, the operation of the proposed CAM cell was evaluated using QCADesigner tool. In addition the proposed design was implemented in a single layer which in general increase its manufacturability and decreases fabrication costs for QCA chip designers when compared to the multi-layer implementations [3].

The rest of this paper is prepared as follows: Section 2 provides preliminaries of QCA and CAM. Section 3 highlights the related works. The details of the proposed design are provided in Section 4. Comparisons and simulation results are presented in Section 5. Finally, the conclusions will be presented in the last section.

2. Preliminaries

2.1 QCA

Each QCA cell has a square shape which has four quantum dots including a pair of electrons. Fig. 1 illustrates the primary QCA cell. As a result of the columbic interaction between the electrons, the dots will be filled diagonally. The polarization of energy (P) in each cell can be calculated using Eq. (1) where pi is the probability of the presence of an electron at the quantum dot i.

$$p = \frac{(p1+p3)-(p2+p4)}{p1+p2+p3+p4} \quad (1)$$

The two electrons can change their location through tunneling between adjacent dots depending on the driver cell polarization. There are two configurations of QCA cell whose polarizations -1 (represent logic “0”) and +1 (represent logic “1”) [8].

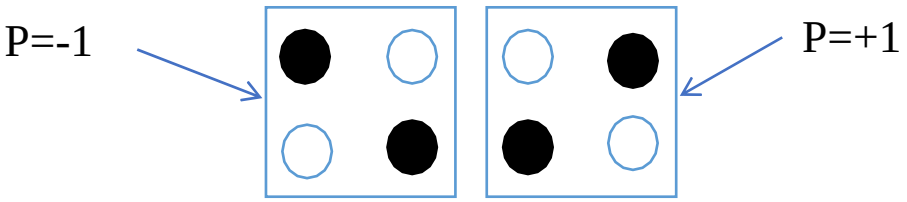


Fig. 1- Primary QCA cell

Each wire in QCA is made up of basic cells that propagate input logic value to the output cell through columbic interactions between the electrons of the array cells. The implementation of this concept is in two types. The first one is common 90^0cells, while in the second 45^0 rotated cells. These two types of QCA wires shown in Fig. 2 [8] used together to bypass the crossover problems to achieve coplanar crossing while [9] reach a new approach.

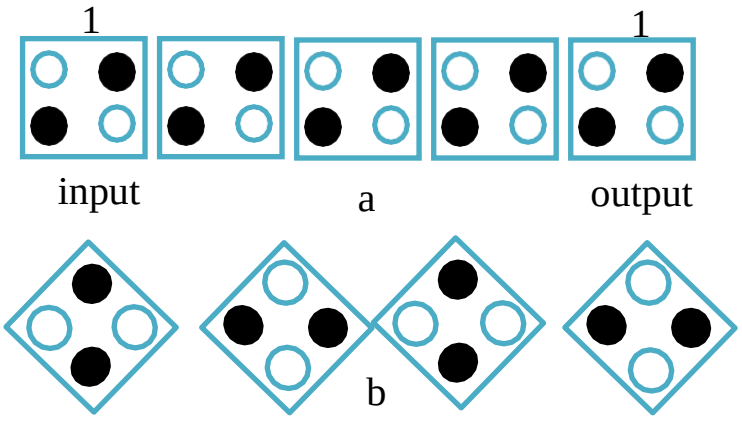


Fig. 2 - QCA wire (a) 90^0 cell; (b) 45^0 cell

In general, there are three forms of the inverter gate in QCA as shown in Fig. 3. If a logical value is applied to the input cell, we will get the inverted value at the output. In addition, the majority gate has attracted the attention of many researchers, where several papers highlighted on it such as [10-14]. The majority gate in QCA is of two types as shown in Fig. 4, where the gate contains three input cells, one voter and one output cell. Many circuits can be implemented using the inverter gate and the majority gate [15]. If a minimum of two inputs in the 3-inputs majority gate is set to "1", the output will be "1" otherwise it will be "0". The functionality of a 3-inputs majority gate is given by Eq. (2) [1].

$$M(A,B,C) = AB + BC + AC \tag{2}$$

we can get 2-input OR gate and 2-input AND gate from the 3-input majority gate by fixing any input cell to logic ‘‘1” and "0" respectively, as shown in Eq. (3).

$$\begin{aligned} M(A,B,0) &= AB + (B0) + (A0) \\ M(A,B,1) &= AB + (B1) + (A1) \\ &= AB + B + A = B + A \end{aligned} \tag{3}$$

From these AND and OR gate, the complex logic circuit can be implemented.

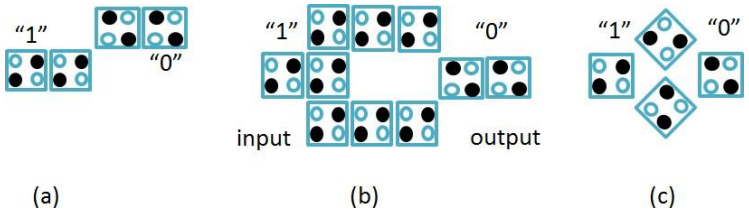


Fig. 3 - QCA inverter forms, (a) Corner approach; (b) Robust design; (c) Rotation

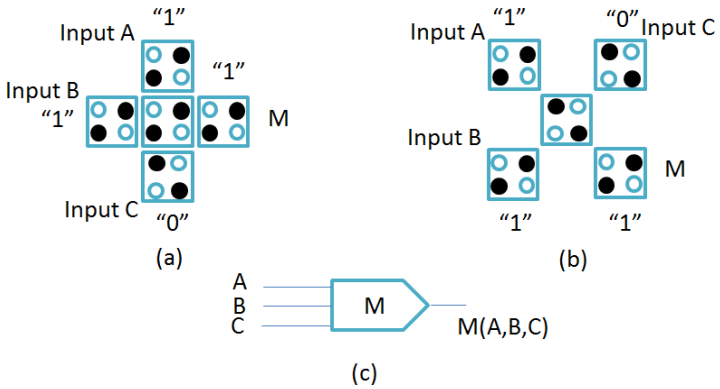


Fig. 4 - QCA 3-input majority gate (a) Ordinary majority gate; (b) Rotated majority gate; (c) Majority schematic

Every QCA based circuit need clock signal for synchronization, control flow and provide power to stimulate the circuit. The synchronization is done by a clocking signal which can be achieved by controlling the potential barriers between adjacent quantum dots. When the potential is weak, which means that there is no clear polarization of the cell. As the potential barrier rises, the result is a reduction in the tunneling rate so that the electrons start to get localized. Once the electrons are localized, the cell gets a specific polarization. The cell will be latched when the potential barrier gets its highest value, the latched cells are represented as virtual inputs. As a result, actual inputs begin to receive new values. This facilitates the ease of pipelines of QCA circuits. Each $\pi/2$ degree for clocking zones out of phase is all that required by any QCA circuit as shown in Fig. 5 [5].

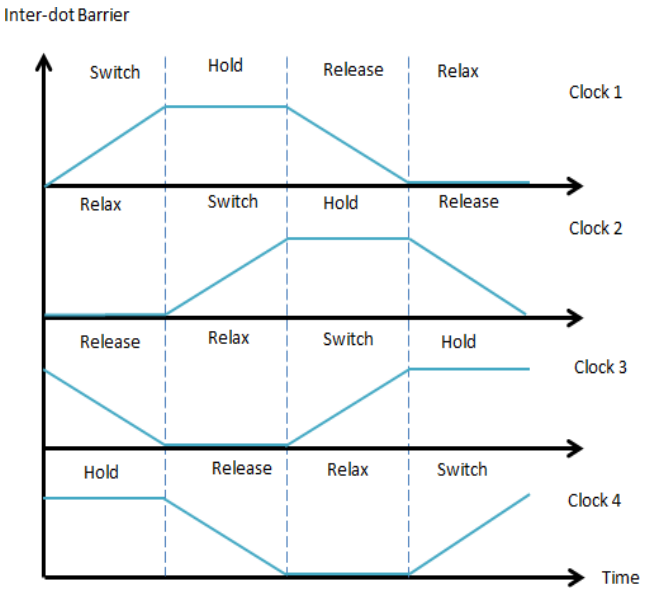


Fig. 5 - The four-phase clock signal and its four different zones

During the switch phase, the depolarized cells are polarized depending on the state of adjacent cells. Actual computation takes in this clock phase. During the hold phase, the second, the change of polarization is impossible. In the Release phase, the third, cells can relax to depolarized state. Finally, during the Relax phase, the fourth phase, cells remain in the depolarized state. the data flow path in QCA depends on the path where clocking phases increase. In QCA, the control of data flow is a specific feature that did not exist in traditional CMOS. This inherent property helped the designers in developing more novel structures for digital circuits [5].

2.2 CAM

CAM is a special type of memory where data is accessed via its content. CAM is able to search its total contents by only one clock cycle [16]. It is also known as associative storage, associative memory, or associative array. The time needed to find an item can be greatly reduced if we know its content compared to detecting it by its address. Because they are an associative memory, they are closely correlated with parallel searches by associating data. In CAM, each location contains logical circuits and storage capacity, as shown in Fig. 6(a) and (b). The operation of a CAM, in summary, is to pick a word needed as a key and return its memory location as a result [3].

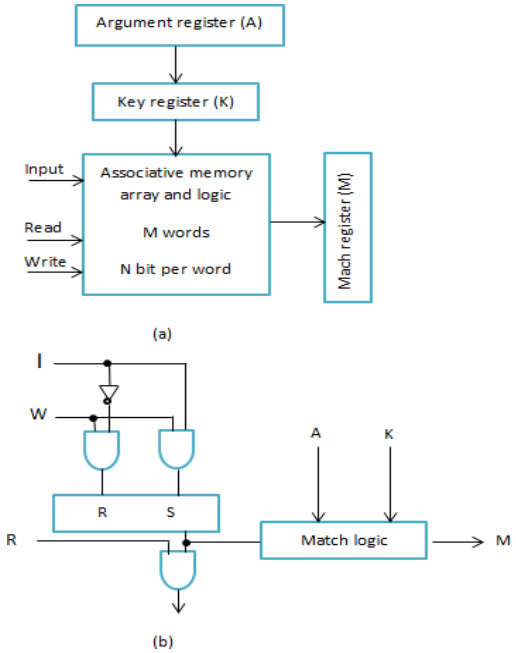


Fig. 6 - Block diagram of (a) organization of CAM; (b) internal organization of a typical CAM cell

3. Related Works

3.1 Five input majority gate

The majority gate with five-inputs in QCA technology is one of the most substantial elements, which can be employed effectively for implementing arithmetic and logic circuits and memory elements such as CAM cells. The operation of the majority gate with five-input can be expressed according to Eq. (4). The truth table is given in Table 1 [1].

$$M(A,B,C,D) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (4)$$

Table 1 - truth table of 5- input majority gate

∑(A,B,C,D,E)	Maj(A,B,C,D,E)
0	0
1	0
2	0
3	1
4	1
5	1

Generally, the majority gate with 5-input produced with five input cells, one output cell, and voter cells. Fig. 7. shows four important majority gates with 5-inputs. In the design shown in Fig. 7 (a), the input cells are placed contiguously and very close to each other, which limit their extendibility [17], while the design is shown in Fig. 7 (b) has many limitations in the position of the output cell, where it is placed in the gate center [18]. If this majority gate is used in a design, the design cannot be done with a single layer. So as to overcome the mentioned disadvantage, a design has been proposed in [7], which is shown in Fig. 7 (c). Nevertheless, in order to implement this design, more cells and more area are needed. In addition some fault-tolerant majority gates with 5-input have been proposed such as in [19] and [20]. These designs are implemented using a higher number of cells and a very large area [1].

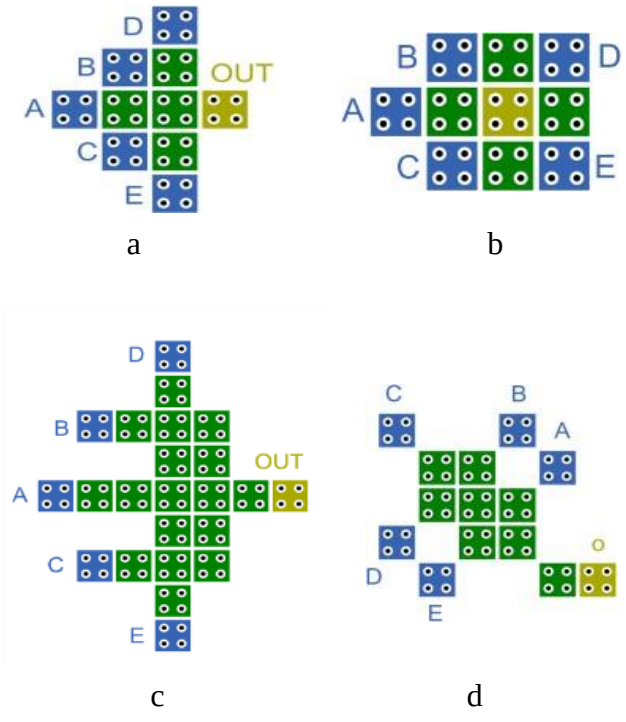


Fig. 7 - Important majority gates with 5-inputs (a) [17]; (b) [18]; (c) [7]; (d) [8]

3.2 QCA CAM cell based on 5-input majority

CAM memory use the content to access the data instead of the address. The CAM is applied particularly in very-high-speed searching applications. The schematic CAM is illustrated in Fig. 8. In CAM, input data is compared with data array stored in a parallel way, and the corresponding address is returned. CAM design based on QCA is illustrated in Fig. 9. [3]. This design is based on a majority gate with five-input which was previously presented in [3] and [1]. This construction consists of two main components. The first one is a memory unit and the other is the matching unit [1].

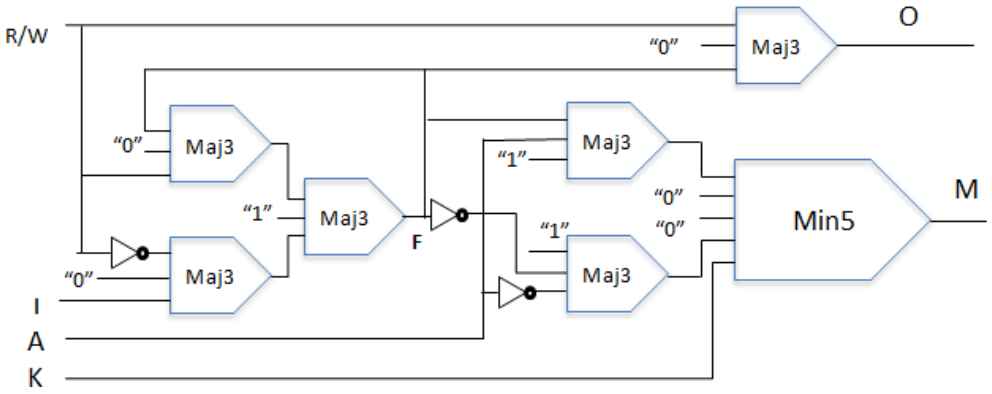
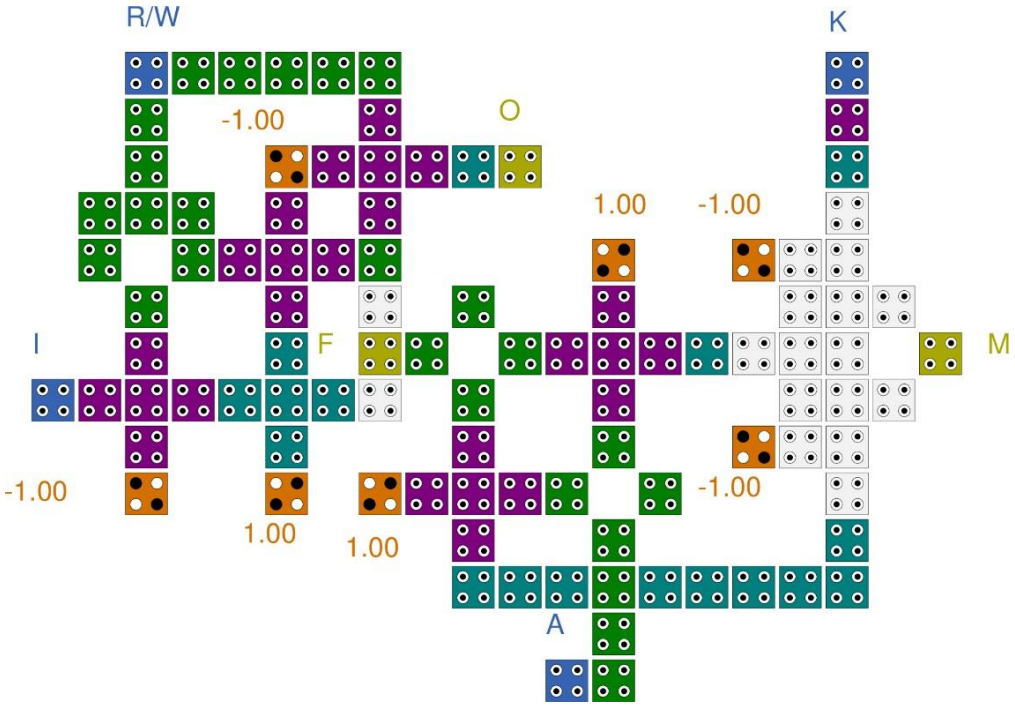
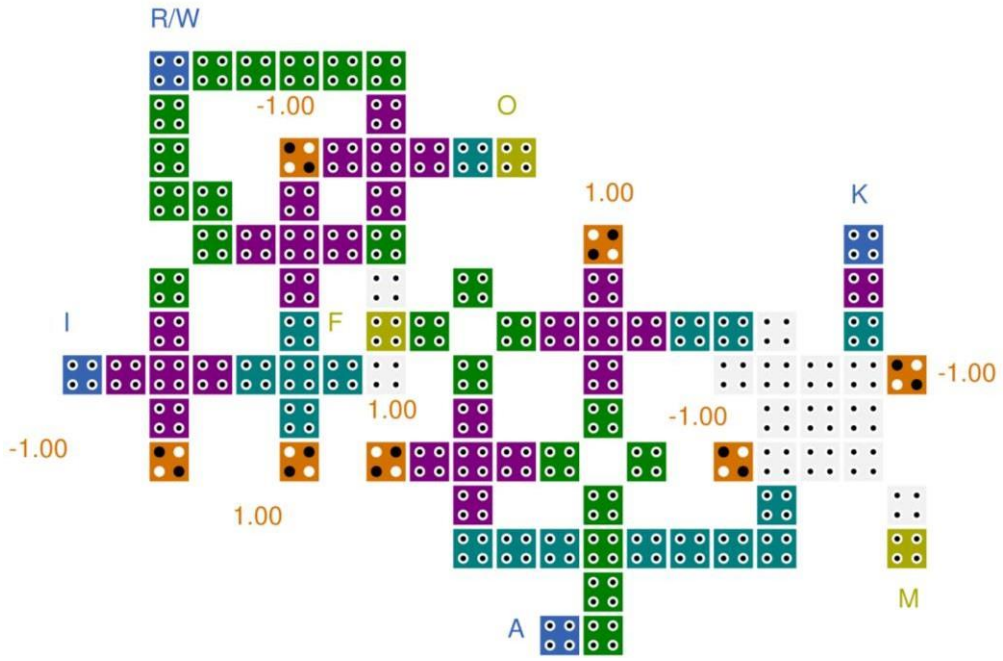


Fig. 8 - CAM cell structure Proposed by [3]

The memory unit consists of (read/write) signal and data input. The matching unit gets the content of the memory cell (indicated as F) with the argument (indicated as A) and key signals (indicated as K). This construction gives an output (indicated as O) as the cell content where the data have been read and sets the match signal (indicated as M) if the data is existed [1].



(a)

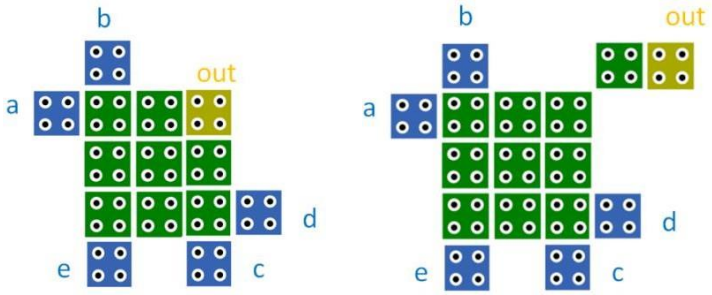


(b)

Fig. 9 - Previous majority gate with five-input -based CAM (a) presented in [3]; (b) presented in [1]

4. The Proposed Design

A majority gate with five-input is proposed in this section, from this gate we can derive the minority gate easily by putting the inverter on the output. Based on these components, a new CAM cell is introduced. Fig. 10 shows the layout of the proposed QCA majority gate with five-inputs. The majority gate with five-input proposed in this work consists of five cells as inputs, 8 cells as a voter and one output cell. The proposed design provides a superior preference for many figures of merit and reduces the constraints that were imposed on previous designs to a large extent. The major advantage of this gate is it can be implemented in a single layer which reduces the complexity of large circuits and enhances its manufacturability. The square layout of the proposed gate lets it better manage its physical design.



(a) (b)

Fig. 10 - (a) Proposed majority gate 5-input; (b) minority gate 5-input

Fig. 10 shows the proposed gates (majority and minority). The proposed minority gate will be used in the CAM cell circuit by following Fig. 8 to carry out final QCA-CAM cell as shown in Fig. 11. This CAM comprises six 3-input majority gates and one 5-input minority gate. Tables 2 and 3 illustrate the truth tables for the memory operation and the matching unit. Consequently, when the Read/Write (R/W) signal is set to "0", the data input will be moved to the output F, thus, the write operation will be performed.

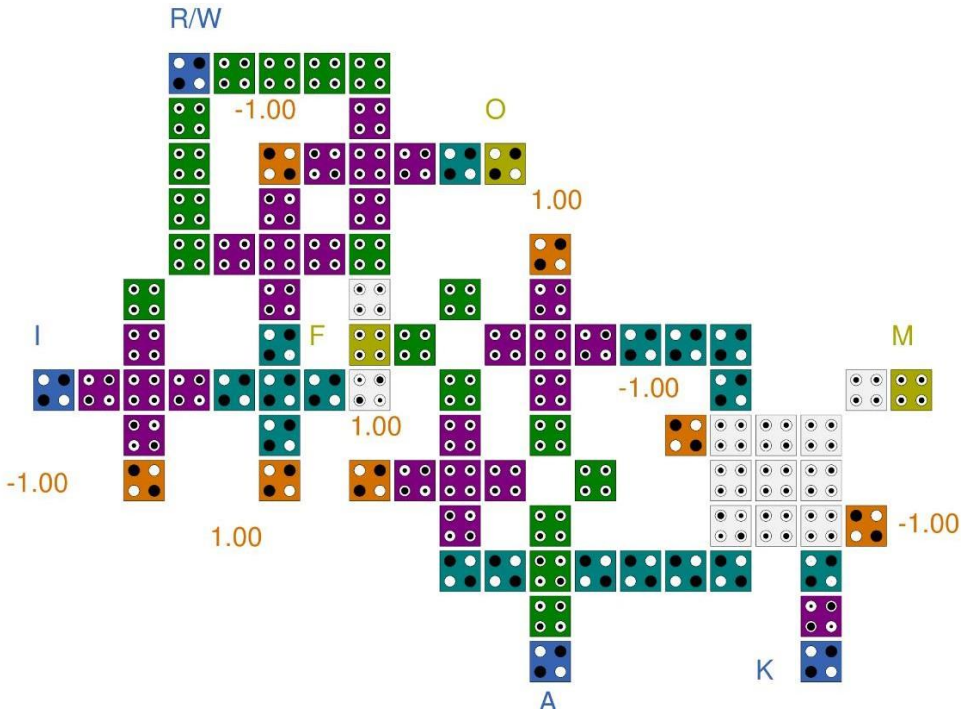


Fig. 11 - Proposed CAM cell structure

Additionally, if R/W is set to "1" the read operation will be performed where the last value of F is transferred to both output F and O. If K signal is set to “0”, the matching signal M will be set to “1”. However, if K signal is set to “1” and the values of A and F are equal, the M signal will be set to “1”, and if the values of A and F are unequal then the M signal is set to "0" [1].

Table 2 - Memory operation truth table [1]

Operation type	R/W	I	Previous F	F	O
Write	0	1	x	1	0
Write	0	0	x	0	0
Read	1	x	1	1	1
Read	1	x	0	0	0

Table 3 - Matching operation truth table [1]

K	A	F	M
0	X	X	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

5. Simulation result and comparison

In this section, the proposed design is evaluated using QCADesigner tool v 2.0.3 without changes in default values. The QCA cell size is set to 18×18 nm where the diameter of quantum dots is set to 5 nm. Fig. 12 shows the simulation result of the proposed majority gate with five-input, which indicates the correct operation of the proposed design. The comparisons between the proposed majority gate with five-input and its most efficient similar gates are given in Table 4. The design presented in [14] although it is a single layer design, it has a cross talk effect when applying the input and this will cause an error in the output.

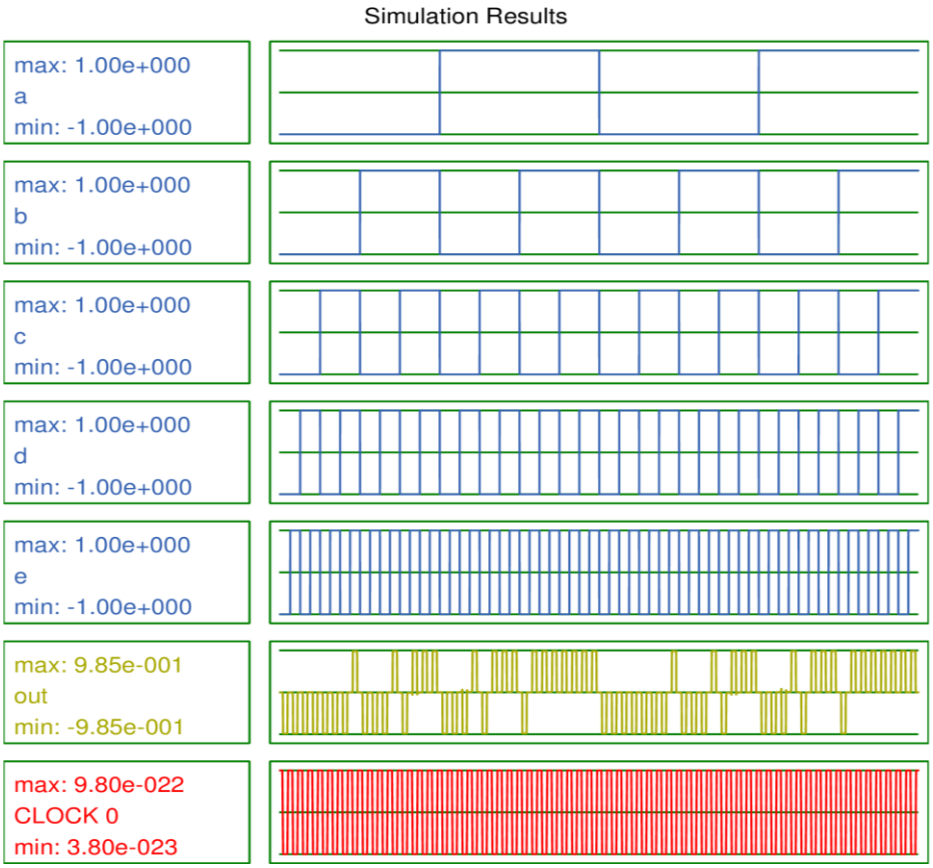


Fig. 12 - Simulation results of majority gate with five-input.

Table 4 - The characteristics of the majority gates with five-inputs

Five-input majority gate	Area (μm^2)	Numbers of cells	Layer Type
[17]	0.01	10	Single
[18]	0.005	10	Multiple
[7]	0.02	23	Single
[20]	0.03	42	Single
[19]	0.04	51	Single
[1]	0.01	17	Single
[21]	0.02	18	single
proposed	0.01	14	Single

Fig. 13 shows the simulation results of the proposed majority gate-based CAM cell. The simulation results verified the right operation of the proposed design. In addition, Table 5 compares the results of the previous work which used 5-input majority gate-based CAM cell with the proposed design. From the layout and simulation output, we can see that the proposed gate is error free and has effectively reduced the previous complexity and the number of cells used.

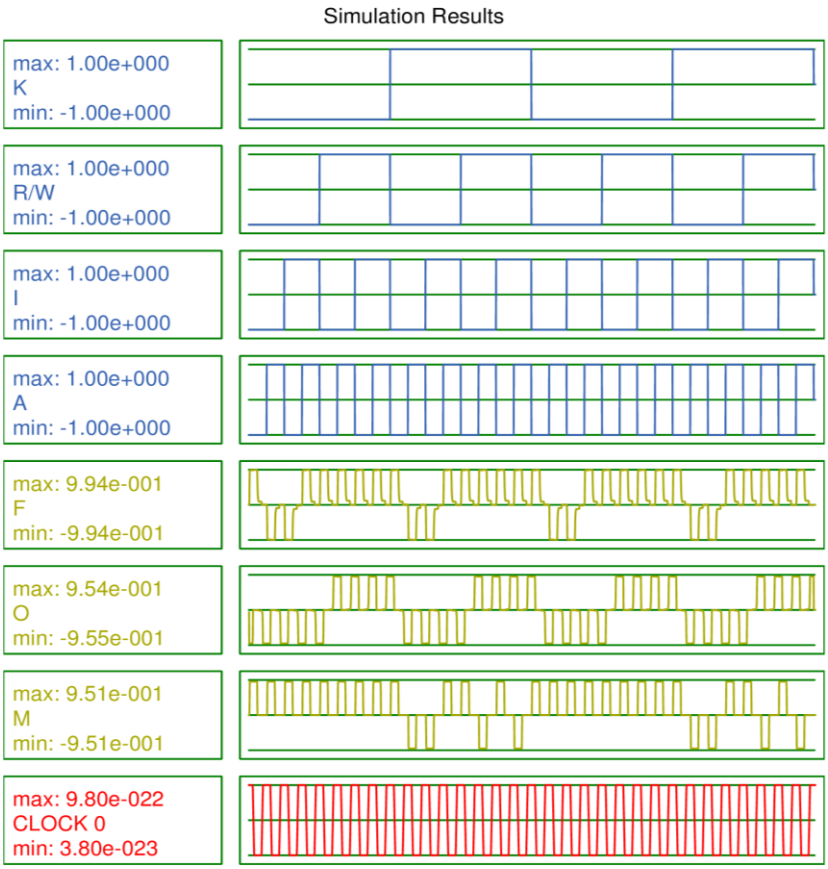


Fig. 13 - Simulation results of the proposed CAM cell Table 5 -

The characteristics of the CAM cells

CAM cell	Numbers of cells	Area (μm^2)	Latency (clocks cycles)
[3]	100	0.14	2
[1]	94	0.11	2
Proposed	87	0.11	2

6. Conclusions

In this paper, a novel structure for 5-input majority gate with QCA has been introduced. The presented gate is compared to the previous designs and its clear from the comparison that the proposed gate solves the cross-talk problem in the best previously reported design. CAM memory with QCA technology is discussed in this work and the proposed 5-input majority gate is developed to 5-input minority gate and then used to design the CAM cell. The CAM cell designed in this work shows good performance as demonstrated from the output waveforms obtained from the simulation tool and reduce the complexity by 7% in terms of the number of cells compared to previous designs.

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