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Effects of High-k Dielectric Materials on Electrical Performance of Double Gate and Gate-All-Around MOSFET

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Abstract: This paper presents the electrical behaviour of Double Gate (DG) and Gate-All-Around nanowire (GAA) MOSFET using different high permittivity (high-k) gate dielectric materials. In order to study the influence of high-k dielectric material towards DG and GAA, Atlas Silvaco TCAD tools were used to simulate the device and to determine the electrical characteristics. The high-k materials chosen in this study were Silicon Nitride (Si3N4), Aluminium Oxide (Al2O3), Zirconium Oxide (ZrO2) and Hafnium Oxide (HfO2). The gate dielectric materials have played a significant role in the design of novel and high performances at nanoscale of electrical devices. It can be observed that when approaching a higher value of dielectric constant, the on current increases while the subthreshold slope (SS) threshold voltage (Vth) and leakaga current reduced. It can be observed that HfO2 shows the best performance compared to other simulated dielectric materials for both DG and GAA MOSFET.

Keywords: High-k dielectric, Double Gate MOSFET, Gate-All-Around MOSFET

1. Introduction

Recently, the miniaturization process of electronic components including transistors in integrated circuits becomes one of the main objectives in semiconductor industry. The purpose of this process is to locate more components per unit area whilst improving the performance of the device itself. Even though making the size of components smaller gives a better resolution, there will always be drawbacks arising during the CMOS scaling process. One major weakness is short channel effects (SCE) that eventually degrades the device performances. However, recently multigate transistor has been proposed to replace the planar MOSFET in order to reduce the SCE. Double Gate (DG) and Gate-All-Around (GAA) nanowire MOSFET are among the multigate transistors which potrays a good role to replace the classical MOSFET due to their ability to suppress SCE (Jena et al. 2016; Tanushree Debilata Das et al. 2017; Chowdhury et al. 2016).

Besides that, the continuous scaling of the physical dimension also leads to another problem which is high leakage current that results in high power consumption. As mention in the International Technology Roadmap for Semiconductors 2.0 (ITRS) 2015 ("International Technology Roadmap for Semiconductor 2.0" 2015), the crucial thing to be taken care of in high-performance device is the power consumption. Previous research has introduced the using of high-k dielectrics as replacement of current gate which is Silicon Dioxide, SiO_2 as gate dielectric film helps to improve the leakage current and to have a better current drive. Previous study shows that high-k materials are more suitable than the SiO_2 due to ability to improve leakage current while having smaller thickness of insulator (El, Hadri, and Patanè 2016).

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Several materials have been investigated as replacement for gate dielectrics instead of SiO_2 such as Silicon Nitride (Si_3N_4), Aluminium Oxide (Al_2O_3), Aluminium Nitride (AIN), Lanthanum Oxide (La_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2). These materials are chosen because they are thermodynamically stable in contact with silicon and have higher permittivity as compared to SiO_2 (Dueñas et al. 2012). This paper presents the study of using different high-k dielectrics and their impact towards current-voltage characteristics, on current, off current, Ion/Ioff ratio, Vth and SS.

2. Device Structure and Simulation

The cross-sectional views of DG and GAA nanowire are illustrated as in **Fig 1 (a)** and **(b)**. The blue colour is the oxide layer which is SiO_2 that will be change later to other high-k materials. The orange colour represents the channel (silicon-type), the purple layer is the conductor layer and red colour in GAA diagram is the polysilicon. The device simulations were performed using Atlas simulator in Silvaco TCAD tool. Both of DG and GAA are having the same parameter setting as shown in **Table 1**. In this study, SiO_2 is replaced with other different high-k dielectric materials. The high-k materials chosen in this study are Si_3N_4, Al_2O_3, ZrO_2 and HfO_2. **Table 2** shows the band offsets and dielectric constant for different dielectric materials (Chaudhary et al. 2018),(V. Kumar et al. 2011) used in this simulation.

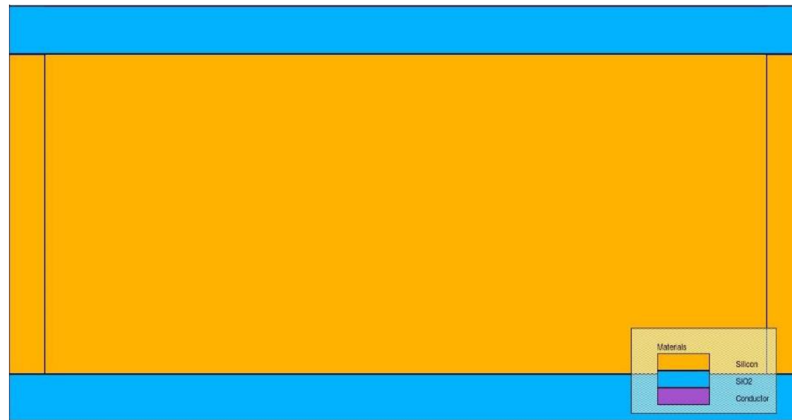
Table 1 - Physical parameter setting for simulation structure.

Parameter	Value
Oxide thickness, t_{ox}	1.5 nm
Silicon film thickness, t_{si}	10 nm
V_{DD}	1V
Substrate concentration, N_A	$1x10^{15}$ cm^{-3}
Drain and source concentration, N_D	$1x10^{20}$ cm^{-3}
Channel length, Lg	1 µm

Table 2 - Properties of different high-k dielectric materials

Material	Dielectric Constant, κ	Band gap (eV)
SiO_2	3.9	9
Si_3N_4	7.9	5.3
Al_2O_3	10	8.8
ZrO_2	23	5.8
HfO_2	25	6

(a)



(b)

Fig. 1 - (a) Cross-section of GAA; (b) Cross-section of DG

3. Results and Discussion

3.1 Double-gate MOSFET

In this simulation, gate dielectric SiO_2 was replaced by the chosen high-k dielectric materials which are Si_3N_4, Al_2O_3, ZrO_2 and HfO_2. In order to study the effect of using high-k, the results obtained for high-k dielectric materials werethen compared to the result when using SiO_2 as gate dielectric. **Fig. 2** shows the Id-Vgs curve for DG when using different high-k dielectrics materials. It can be seen that HfO_2 has the best transfer characteristic which is high on current followed by ZrO_2, Al_2O_3, Si_3N_4 and SiO_2 respectively. From the graph shown, it is evident that use of high-k dielectrics can improve the transfer characteristic. The results also have a good agreement with previous studies (V. Kumar et al. 2011; Chaudhary et al. 2018; Charles Pravin et al. 2016).

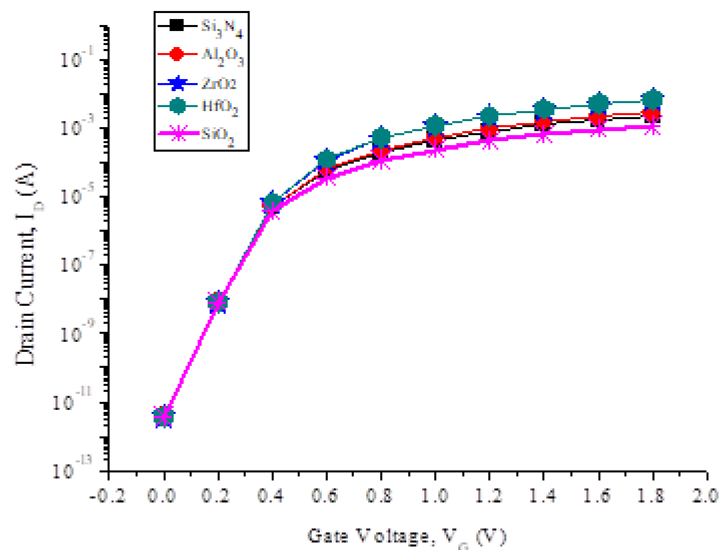


Fig. 2 - Id-Vgs characteristic of DG for different dielectrics constant values at V_{DS}= 1.0V

Fig. 3 represents the off current for DG MOSFET. It can be observed that the leakage current decreases exponentially when approaching higher dielectric constant value. The decrease in off-state current is basically because of the increasing of barrier potential faced by the carriers. Low off-state current leads to higher Ion/Ioff ratio. Ion/Ioff ratio is used to bench mark the devices. If the device shows higher Ion/Ioff ratio it is suitable for high-speed logic and low power applications (Magnusson 2011).

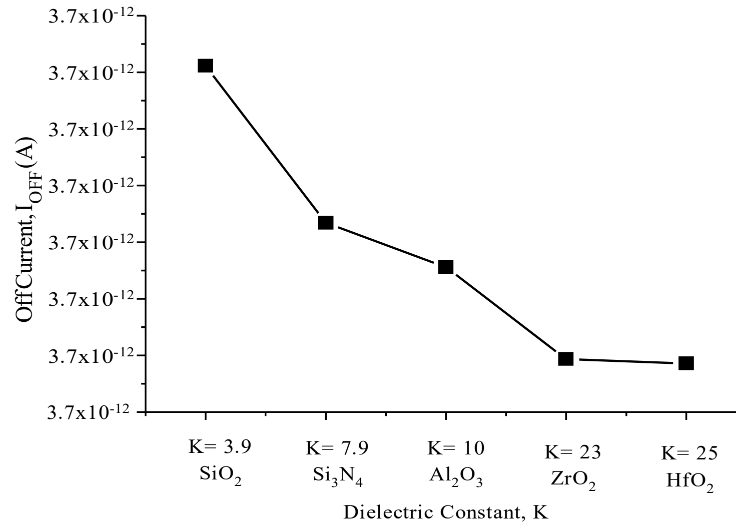


Fig. 3 - Off current for different k values for DG

3.2 Gate-All-Around MOSFET

In the second part, the simulation proceeds with GAA MOSFET with the same step as DG MOSFET. Fig. 4 shows the Id-Vgs curve when different high-k dielectric materials are used. The result of high-k materials are also being compared to SiO_2. For GAA, the trend of the curve is similar with DG but it has lower on current. HfO_2 also shows the best characteristics compared to other materials. As mention before, high-k material will directly cause the on-state current increased and the off-state current reduced due to the increase of fringing electric field. Fig. 5 shows the variation of leakage current with respect to different gate dielectric materials and exhibits an effective suppression for all the gate dielectric materials. Basically, SiO_2 is replaced with higher k dielectric materials to avoid direct tunnelling when the tox used is less than 2nm (Robertson and Wallace 2015). Hence, when higher k is used to replace SiO_2, same capacitance but with lower tunnelling current can be achieved.

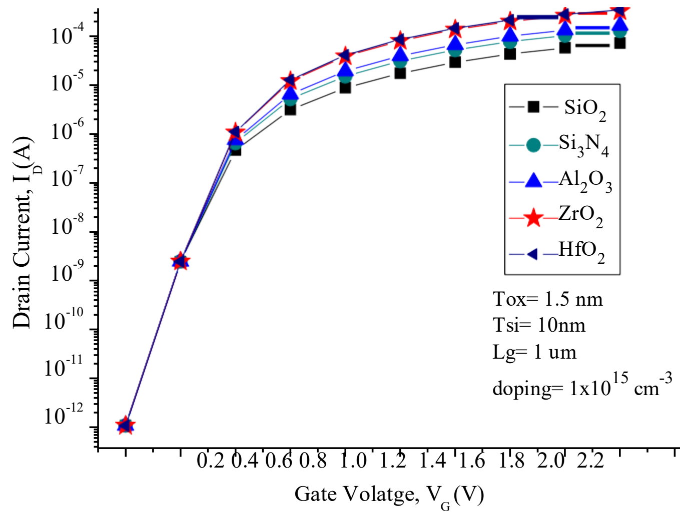


Fig. 4 - Id-Vgs characteristic of GAA for different dielectrics constant values

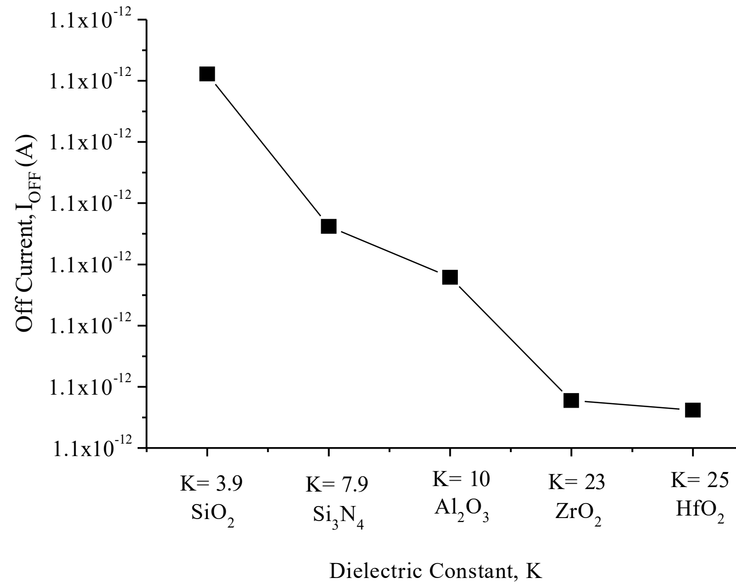


Fig. 5 - Off current for different k values for GAA

3.3 Effect of High-k Dielectric Materials in DG and GAA Towards Vth and SS

The characteristics of DG and GAA were compared to analyse which transistor is having better performance in terms of Vth and SS when high-k dielectric material is used in the simulation.

Fig. 6 shows the comparison of on state current for DG and GAA with various dielectric constant values. On state current is also one of the important parameters of a device, which determines fan out and fan in capabilities of a circuit. The on current increased when the gate oxide is replaced with higher dielectric constant material compared to SiO_2. This is because the used of high-k material increase the fringing electric field in the device. Hence, the on state current will increase while reducing the off-state current (Tripathi, Mishra, and Mishra 2012). However, very large value of high-k (k>25) is not really good for suppression of short channel effects since stronger fringing fields will induce electric fields from source/drain to the channel thus results in degradation of gate control (Mohsenifar and Shahrokhabadi 2015). Result shows that DG has higher on current ratio compare to GAA. The increase in dielectric constant results in enhanced gate oxide capacitance and hence better gate control. Fig. 7 shows the SS characteristic for DG and GAA respectively. Both devices show that the SS is lower when higher dielectric constant is used. The lower the value of SS, the more efficient and rapid the switching speed of the device from the off state to the on-state current. Here it is proven that having high-k material will help to suppress SCE and hence improve the device performance. Both GAA and DG is favorable since it has nearly-ideal SS which is 60mV/dec.

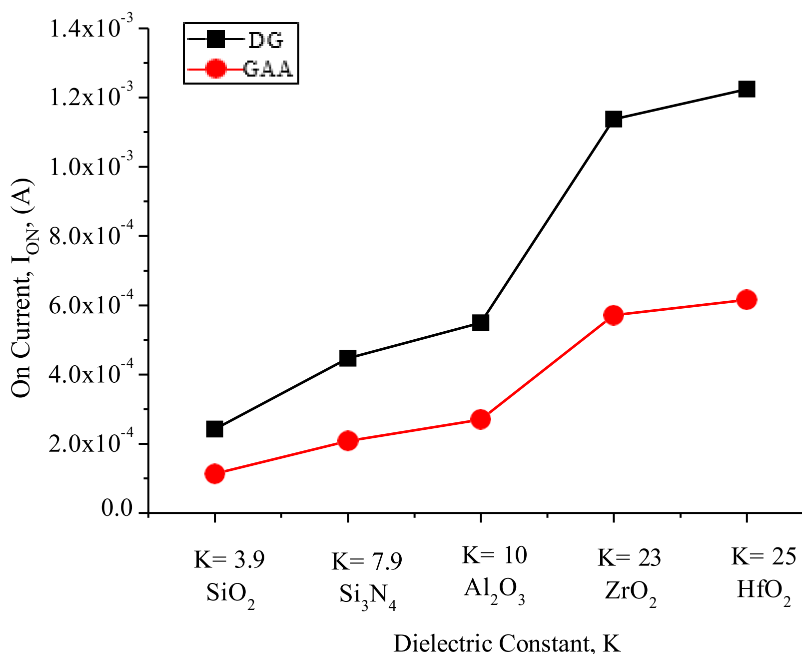


Fig. 6 - The comparison of on current for DG and GAA

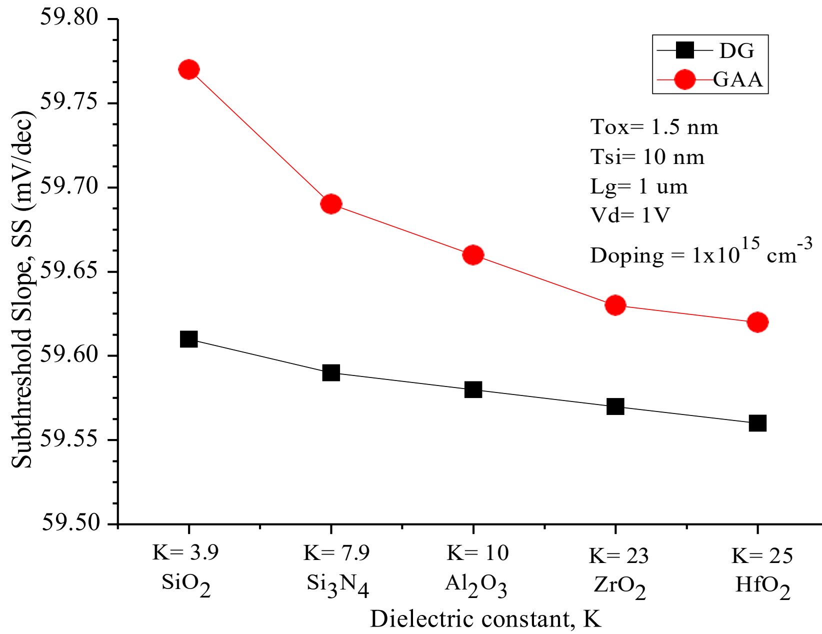


Fig. 7 - SS variation for different gate dielectrics for DG and GAA

Fig. 8 shows the characteristic of Vth with the variation of high-k dielectric material for DG and GAA MOSFET respectively. Both devices exhibit similar trends which is with the increase in dielectric constant the threshold voltage of the MOSFET decreases (Dhariwal and Singh 2016) (El, Hadri, and Patanè 2016). SiO_2 has highest value of Vth for both DG and GAA.It is well-known that high-k materials are more suitable than the well-known SiO_2 due to the smaller thickness required which decreases the threshold voltage and improves the leakage characteristics of the device.

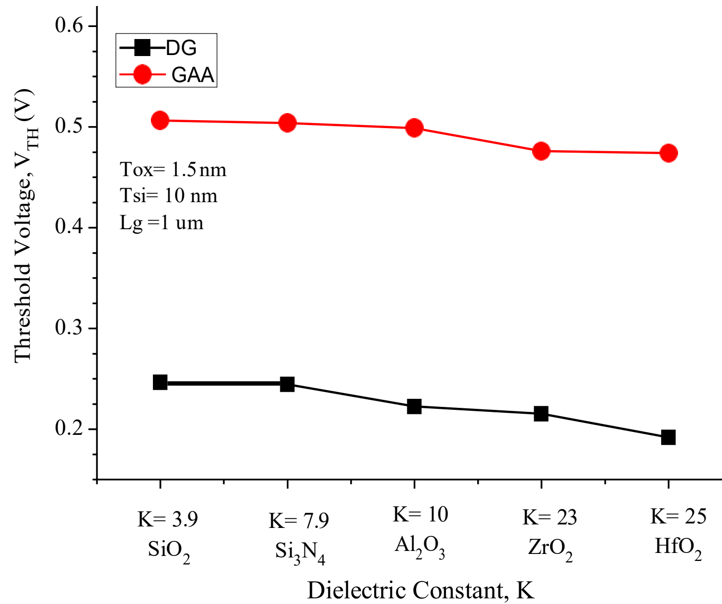


Fig. 8 - Vth with increasing dielectric constant between DG and GAA

3.4 Process Variability Analysis of SiO2 and HfO2 towards Vth, SS and Leakage Current

In this section, scaling the physical dimension such as channel length, oxide thickness and channel thickness were applied in order to study their interaction towards their electrical parameter. Besides that, the simulation also focuses on the use of two different types of dielectric materials which are HfO_2 and SiO_2 to see the effects towards the electrical behavior.

Table 3 shows the variation of silicon film thickness towards SS and leakage current using two different types of dielectric material in DG and GAA MOSFET. It can be observed that, HfO_2 has lower leakage current compared to SiO_2 even though the silicon thickness is approaching 5 nm. It shows that HfO_2 has smaller SS at tsi 20 nm even compare with the SS for SiO_2 at 15nm for both DG nad GAA. This verifies the fact that the use of high-k is able to reduce the short

channel effects (SCEs) (Chatterjee, Chattopadhyay, and Taki 2018). For GAA, SS for higher k dielectric is better due to better gate coupling given by the high-k dielectric.

Table 4 show the effect of variation of channel length towards Vth and leakage current. Both DG and GAA exhibit the same pattern in which the Vth is increasing when approaching 100 nm channel length which in turn results in the decreasing of off-state current. At 30 nm, DG has higher leakage current when using SiO_2 as dielectric compared to HfO_2. 30 nm is so thin that electrons can directly tunnel through the oxide, resulting in excessively high gate leakage current. However for GAA, the leakage current for HfO_2 is not increasing as it proves that using high-k material really helps in improving leakage current while approaching narrow channel length (R. Kumar and Mehra 2016).

Table 3 - Channel thickness vs subthreshold slope and leakage current for DG at Lg=100nm

Channel Thickness, Tsi (nm)	DG				GAA			
	SS (mV/dec)		Ioff (A)		SS (mV/dec)		Ioff (A)	
	SiO_2	HfO_2	HfO_2	SiO_2	SiO_2	HfO_2	HfO_2	SiO_2
5	59.87	59.67	4.77E-08	5.52E-08	59.63	59.56	2.52E-13	2.54E-13
10	60.24	59.85	1.08E-07	1.34E-07	59.78	59.62	1.08E-12	1.09E-12
15	60.81	60.13	1.88E-07	2.46E-07	59.94	59.71	2.42E-12	2.45E-12
20	61.72	60.56	2.98E-07	4.16E-07	60.10	59.82	4.52E-12	4.57E-12

Table 4 - Channel length vs Vth leakage current for DG and GAA

Channel Length (nm)	DG				GAA			
	Vth (V)		Ioff (A)		Vth (V)		Ioff (A)	
	HfO_2	SiO_2	SiO_2	HfO_2	HfO_2	SiO_2	SiO_2	HfO_2
30	0.20	0.14	2.59E-07	3.52E-09	0.32	0.34	3.24E-10	8.47E-11
60	0.43	0.39	2.28E-10	1.13E-10	0.41	0.45	3.31E-11	2.45E-11
100	0.44	0.41	6.39E-11	4.94E-11	0.46	0.49	1.45E-11	1.25E-11

4. Conclusion

By using Atlas Silvaco TCAD tool, device design model and the simulation were performed to evaluate the electrical characteristics for DG and GAA MOSFET by using different gate dielectric material. It can be observed that towards higher value of dielectric constant, the on current and Ion/Ioff ratio, will increase while the SS, Vth and leakage current will reduce. An increased value of dielectric constant improves electrical device characteristics. Overall, HfO_2 shows the best performance compared to other simulated dielectric materials especially with SiO_2 for both DG and GAA MOSFET even in smaller dimension. GAA has better leakage current, SS characteristics when using higher k material while DG has better Vth characteristics.

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Author's Note

The authors declare that there is no conflict of interest regarding the publication of this article. Authors confirmed that the data and the paper is free of plagiarism.

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