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High-Performance Bootstrapped Sample & Hold Circuit for ADCs: Achieving Low Power and Enhanced SNR/SNDR in 45nm CMOS Technology

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Abstract

A sample and hold (S/H) system is commonly used alongside Analog to Digital Converters (ADCs) to accurately convert analog signals into digital form. This paper presents a low-power bootstrapped S/H circuit designed to improve signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR), and power efficiency in both low and high-frequency applications. By charging the bootstrap capacitor through a connection between the transistor's source and body, the input range is increased, which lowers power consumption without affecting the SNDR. The proposed design, developed using the bootstrapped method, maintains the functionality of the sample and hold circuit while boosting the differential input signal amplitude to 300mV in 45nm CMOS technology. The design demonstrates minimal power consumption of 0.21, 0.027, and 0.23µW, while achieving higher SNR values of 72.43, 66.79, and 77.57dB at 50, 100, and 500MS/s, respectively. Additionally, the SNDR shows improved values of 52.47, 52.95, and 51.22dB at those same sampling rates. The proposed bootstrapped S/H circuit was simulated using LT Spice IV in 45nm CMOS technology.

1. Introduction

As the number of mobile devices and wireless networks continues to expand exponentially, the demand for more efficient integrated circuits has become a critical concern [1, 2]. For accurate reconstruction of continuous analog signals at the receiving end, an analog-to-digital converter (ADC) is essential. ADCs convert analog signals into discrete digital data for processing, transmission, and delivery. Essentially, ADCs are electronic devices or circuits that transform continuously varying analog signals into digital representations, enabling processing by digital systems such as microcontrollers, computers, or digital signal processors [3, 4]. A crucial component of analog building blocks, especially in ADCs, is the sample and hold (S/H) circuit [5]. The performance of data converters can be significantly influenced by the front-end S/H circuit, as it helps reduce errors caused by small variations in delay times during the internal operation of the converter [6]. The bootstrapped switch examined in this study is

suitable for resolutions ranging from 8 bits to 11 bits, though higher resolutions above 12 bits and high sampling rates are not recommended for driving loads with substantial capacitance [7] [8]. However, in extreme radiation environments—such as space missions, aircraft, and nuclear fusion reactors—ADCs can experience significant degradation in functionality, especially in their sub-block circuits. This poses considerable challenges in managing such systems effectively [9]. The S/H circuit is critical in ADCs as it allows the conversion of sinusoidal signals into discrete signals. In ADC circuits, the sample and hold stage uses a switch to rapidly sample the analog signal at specific intervals. Without a front-end sampling network, the performance of the entire converter can significantly decline, particularly with high-frequency input signals [10]. In A/D architectures, the input waveform can be sampled within the converter or in a dedicated input S/H circuit. Using a capacitor, the sample and hold circuit "holds" the voltage value that was sampled, effectively isolating the sampled value from further changes in the input signal, thereby stabilizing the conversion process [11].

A bootstrapped sample-and-hold circuit can reduce the impact of the sampling switch's on-resistance on the input voltage, thus improving the circuit's linearity [12, 13]. However, the input signal's magnitude is limited due to voltage stress on the gate oxide of the sampling switch during the sampling phase, caused by the sum of the input signal's peak voltage and the bootstrap (Gate-to-Source) voltage. Prolonged voltage stress can damage the gate oxide, diminishing the device's overall reliability [13]. To mitigate this issue, reducing the bootstrap (Gate-to-Source) voltage is suggested, as it decreases voltage stress on the gate oxide during transient events. The sampling transistor switch, linked in series with the bootstrapping circuit, helps make the switch independent of the input signal by lowering the on-resistance between the sampling switch's input and output, thereby improving circuit linearity [14]. As the number of cascade transistors increases, so does the output swing, making basic buffer operation optimal for low voltage supply [15]. A sampling circuit stabilizes the gate-to-source voltage. The main components are the hold capacitor (CH) and the sampling switch (MSW) coupled to the bootstrapping circuit. Bootstrapping reduces the on-resistance between the sample switch’s input and output, thereby improving linearity. During sampling, switches stabilize the gate-to-source voltage by charging a bootstrap capacitor [16]. For holding, the CB capacitor is biased with VB to eliminate voltage across the sampling switch, thereby boosting input voltages. This setup allows the circuit to handle larger input voltages while preventing CB discharge during sampling [12]. Further optimization of the proposed S/H circuits could include improvements in noise reduction, bandwidth enhancement, and real-world implementation to validate their performance [17].

This paper proposes a low-power bootstrapped Sample and Hold Circuit utilizing a three-segment experimentation approach. The proposed design uses a bootstrapped CMOS switch, minimizing unnecessary MOS switches and conserving energy by utilizing only fourteen switches. A bootstrapped switch and three capacitors are used for sampling and holding to obtain precise feedback. In the first experiment, a 300mV input range, 1MHz input frequency, and 50MS/s sampling rate are used. The second experiment increases the sampling frequency to 100MS/s with the same input conditions. In the third experiment, the sampling frequency is raised to 500MS/s, with a 10MHz input frequency and a 300mV input range. This implementation improves SNR and SNDR results without sacrificing the sampling frequency. The proposed circuit effectively addresses the challenges presented by these three-segment trials.

2. Literature Review

Within the BSIM 3v3.1 foundry, a simulation of a sample and hold circuit was carried out employing technology with a 0.18um feature size. The utilization of SPICE parameters yielded a much-improved outcome compared to prior studies. The frequency of sampling is 100MHz, while the input frequency is 2MHz. The provided voltage supplied to the circuit is 1.8V, whereas the full-scale input range, measured from peak to peak, is 1.2V. The power consumption of the device is 6.5 milliwatts. The measurement of the Effective Number of Bits (ENOB) is 10 bits, and the measurement of the Signal-to-Noise and Distortion Ratio (SNDR) is 64.5 decibels. This design is applicable for pipeline ADC [18]. However, a 0.35um poly CMOS technology was used to actualize the sample and hold circuit. A sample and hold unit have a capacitance of 1pF for single-ended loads, while the holding capacitors have a capacitance of 0.5pF apiece. The total current for each case was measured to be 0.6mA. Sinusoidal signals with amplitudes of 1.6 volts (peak to peak) and frequency of 1.7MHz, 20MHz, and 40MHz were applied to both sample and hold circuits. The frequencies observed in the samples were 250MHz and 500MHz. It has been discovered that the signal-to-noise and distortion ratio (SNDR) has increased by a minimum of around 10 decibels in each and every one of the cases[19]. This sample-and-hold circuit design employs a "bilateral bootstrapped CMOS switch" that prioritizes good linearity, fast speed, and the capacity to drive large capacitance loads [20]. A 14-bit, 1-MS/s SAR ADC is the primary intended use for this device. The suggested circuit attempts to overcome the shortcomings of conventional CMOS switches by keeping the input voltage's ON-resistance (RON) constant. CMOS Technology at 180nm from TSMC. The circuit that is suggested can drive a total capacitance of 344pF (172pF on every side) with a sampling rate of 1MS/s. The power supply operates at 1.8V. Therefore, evidence suggests an SNDR of 87dB has been reached [20]. Charge injection, input range, clock feedthrough, and input signal dependent on-resistance are among the MOS switch non-ideals. A simple NMOS switch with an on-resistance can be forced

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to disregard the input signal. This problem can be solved with a complementary topology tool. MOS nonlinearities transistors cause this structure's resistance to fluctuate rapidly with input. This limits bandwidth, causing distortion. A substantial distortion-causing nonlinear component in C1 is caused by larger switches' drain junction capacitance.

The author explains the inaccuracy using the following equation after measuring the overlap capacitance and determining that it is constant [21]:

$$\Delta V = V_{ck} \frac{WC_{ov}}{WC_{ov} + C_h} \tag{1}$$

ΔV= The change in Voltage.
V_{ck}= The clock voltage.
WC_{ov}= The term involves the capacitance.
C_h= Some additional capacitance.

This equation (1) appears to be describing a change in voltage (ΔV) based on the clock voltage (V_{ck}), the overlap capacitance (WC_{ov}) and an additional capacitance (C_h). The overlap capacitance is assumed to be constant.

One of the best options for low-voltage operations is grate bootstrapping, which is the preservation of a steady Gate-to-Source voltage during the sampling phase. It is referred to as advanced clock boosting when the voltages at the gates of the sampling switch MSW (gate to source and gate to drain) stay constant while the sampling phase is in progress [22].

Depending on the voltage differential between the input and CH, the sampling switch MSW in the design works under two situations during the sample phase [23]. The linearity is significantly improved when the gate-to-source voltage stays constant at VB during the sampling phase under the starting condition where Vin < VCH. The roles of the sampling switch MSW source and drain are switched in the second situation, where Vin>VCH. Consequently, the gate-to-source voltage becomes:

$$V_{GS} = V_B - \left|V_{DS_{M_{SW}}}\right| \tag{2}$$

A field-effect transistor (FET), more especially a metal-oxide-semiconductor field-effect transistor (MOSFET), appears to be connected to the equation provided. In a MOSFET, the gate terminal controls the current flow between the source and drain terminals. This voltage is known as the gate-to-source voltage, or V_{GS}. The voltage applied to the base voltage, or gate terminal, which acts as the external voltage applied to the MOSFET gate, is denoted by the symbol V_B. When the MOSFET is in the metal-switching M_{SW} mode, the drain-to-source voltage across it is represented by the value of $V_{DS_{M_{SW}}}$ [23].

A constant gate-to-source voltage may be applied to both sides of the sampling switch MSW by utilizing the suggested input range extension approach, which scales the bootstrap capacitor value by a factor of three. Without appreciably expanding the chip area, this is possible to do [23]. The low power, bootstrapped S/H circuit's ability to increase linearity and lengthen the input signal is demonstrated by this circuit. The bootstrapped capacitor may be scaled down by a factor of three by using this circuit's transistor body and source to omit the discharge during the sampling phase. Ultimately, smaller bootstrapped capacitors were added to this sophisticated bootstrapped circuit to improve linearity and maintain a steady gate to source voltage.

3. Proposed Sample and Hold Circuit

An NMOS switch has a rather narrow input signal range which is mentioned in the introduction. A CMOS switch is utilized to solve this issue. To achieve this, this work needs to set the (W/L) of the NMOS and PMOS switches so that

$$\mu_n C_{ox} (\frac{W}{L})_n = \mu_p C_{ox} (\frac{W}{L})_p \tag{3}$$

When it comes to driving power, both the NMOS and PMOS switch are on par. In 45nm_HP CMOS process, the observed function in Equation (4) :

$$(\frac{W}{L})_p = 4(\frac{W}{L})_n \tag{4}$$

Within the framework of this layout, $L_n = L_p$ so that Equation (5) :

$$W_p = 4W_n \tag{5}$$

In Equation (3)-(5) [24], links the oxide capacitance per unit area (Cox), aspect ratios (W/L), and electron mobility (μn) in n-type (electron) and p-type (hole) MOSFETs. This implies that for n-type transistors, the product of electron mobility and aspect ratio is identical to the product of hole mobility and aspect ratio for p-type transistors. An additional connection is mentioned, which indicates that p-type transistors have an aspect ratio four times greater than that of n-type transistors. The relationship between the widths (W) of p-type and n-type transistors is also explained by the equation, which shows that the p-type transistor's width is four times greater than the n-type transistors. The improvement of MOSFET performance and the maintenance of an efficient and well-balanced integrated circuit design are made possible by these relationships, which are essential to the design of semiconductor devices.

In Equation (6)-(9) [21], when utilizing a basic NMOS switch, the on-resistance R_{on}

$$R_{on} = \frac{1}{\mu_n c_{ox}(\frac{W}{l})(V_{dd} - V_{in} - V_{th})} \tag{6}$$

$$R_{on} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})_p(V_{in} - \left|V_{th_p}\right|)} \tag{7}$$

$$R_{on_C} = R_{on_n} \left\| R_{on_p} \right. \tag{8}$$

$$\text{As } V_{in} \to (V_{dd} - V_{th}), the\ R_{on} \to \infty \tag{9}$$

here,
R_{on} = On-Resistance NMOS
μ_n= Electron mobility in the NMOS transistor.
μ_p = Electron mobility in the PMOS transistor.
C_{ox}= capacitance of the gate oxide per unit area.
$\frac{W}{L}$ = Transistor width to length ratio for MOS devices.

In equation (6)-(9), it is about R_{on}'s actions as V_{in} gets closer $(V_{dd} - V_{th})$. Upon approaching the threshold voltage (V_{th}), the input voltage (V_{in}) causes the on-resistance R_{on} to rise sharply and eventually reach infinity. This phenomenon is common in CMOS transistors close to the threshold voltage and is frequently connected to the change in the transistors' states from off to on in digital circuits. The diminishing difference between V_{in} and the threshold voltage, which results in a decrease in the driving force for current flow through the transistor, is the cause of the increase in on-resistance as (V_{in}) approaches $(V_{dd} - V_{th})$.

The design operates bootstrapped CMOS switch that is arranged differentially. The constant ON resistance of the suggested bilateral bootstrapped CMOS switch, which is independent of input fluctuations, is its unique feature. In addition, the differential architecture allows charge injection to be eliminated regardless of input voltage [24]. In the proposed circuit, some changes have made by eliminating the need for a power-hungry source follower buffer and reducing the size of a capacitor and a transistor without sacrificing output. When compared to the foundational paper, the system output rose thanks to our revised architecture. When operating at low voltage, it is crucial to ensure that the technology's reliability constraints are not compromised. Using a MOS transistor as a switch in low voltage operation comes with its fair share of drawbacks. Due to the decrease in supply voltage, it becomes necessary to lower the threshold voltage of high-threshold transistors. This will cause a significant increase in the sub-threshold leakage current, resulting in distortion of the analog sample and an overall increase in static power consumption. In another approach, high-threshold voltage MOS transistors are employed. This technique has certain drawbacks, as the transistors exhibit high series resistance, resulting in a decrease in speed.

In Fig. 1, this circuit was designed mainly to get the lowest possible operating voltage, specifically for one of the sampling transistors in the S/H circuit. The main goal of a bootstrapped circuit is to increase the on-conductance between the sampling circuit's input and output by reducing the sampling resistor's on-resistance. To support a low-power bootstrapped S/H circuit appropriate for low and high-frequency applications, modifications have been made to this section. Currently, the circuit is running on a single-phase clock Q, which turns on and off the bootstrapped switch M14. The bootstrapped circuit enters the Off phase when Q is low because transistors M15 and M16 discharge from the gate of M14 to the ground. Transistors M7 and M8 are used to apply voltage V_{DD} to capacitor C2 at this step. When the M14 is in the ON phase, this capacitor acts as a battery across the gate and source terminal. M12 and M13 have the responsibility of separating switch M14 from C2 when

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it is charging. The transfer of charge from the battery capacitor C2 onto gate T is made possible when Q is high because M9 pulls down the gate of M13. Following this, M12 and M14 become active. The input voltage V_{in} source, which is displaced by V_{DD}, may be efficiently tracked by the gate of T by using M11. This guarantees that the M14 gate-to-source voltage stays constant irrespective of the input signal. Understanding the connection between source S and gate G is essential for an electronics engineer. The gate G in this case is at $(2V_{DD})$ whereas the source S is at (V_{DD}). It is noteworthy, nonetheless, because $(V_{TS} = V_{DD})$. Latch-up is less common thanks to the link between M8's body (n-well) and its source. Although M11 and M15 improve the circuit's dependability, they are not necessary for its operation. M7 is able to charge C2 during the OFF period thanks to the cooperation of M5, M6, and C1 to construct a clock multiplier.

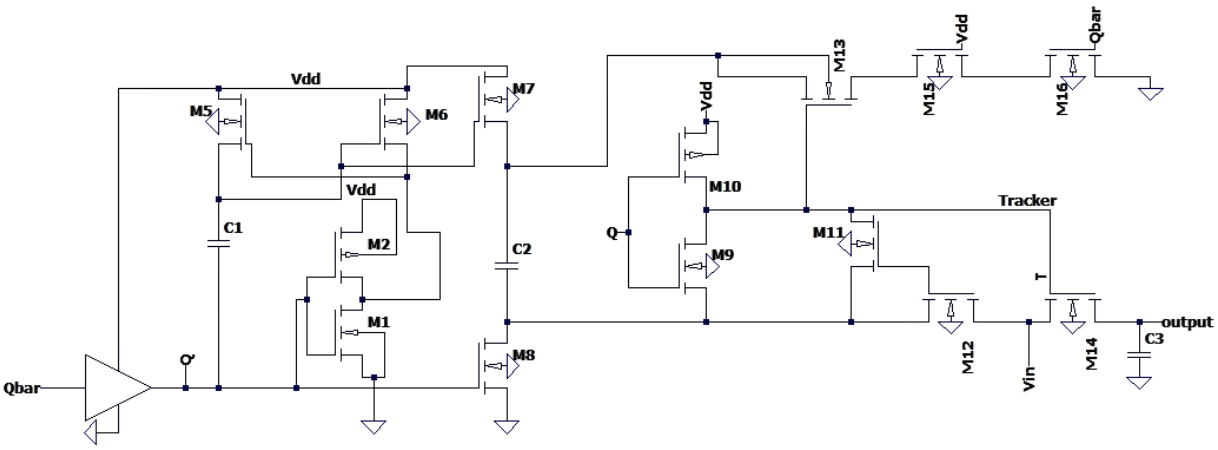

Fig. 1 *Proposed sample and hold circuit*

4. Performance Evaluation

To simulate the given bootstrapped S/H circuit, LT Spice IV was employed, utilizing 45nm CMOS technology. In Fig. 2a, a 300 mVp-p sine wave at 1V supply voltage is the input signal. Input signal frequencies of 1MHz is used for the tests. To convert an analog signal to discrete signal, the procedure of sample and hold plays a crucial role, particularly when the given signal is transposing swiftly that represented at Fig. 2b. In Fig. 2c, it is clearly seen that the sample and hold process is perfectly worked as it is following the sine wave and Fig. 2d portrays the closer view of the whole procedure. The given bootstrapped S/H circuits had their SNDR 52.47 dB and power consumption 0.21µW evaluated. The voltage that was measured at the end of the upgraded low-power bootstrapped S/H circuit is also depicted. In Fig. 3a, a sine wave operating within a 1-volt supply voltage and with a peak-to-peak amplitude of 300 mV is the input signal used to test the supplied bootstrapped Sample-and-Hold (S/H) circuits. For the testing, input signal frequencies of 10MHz are employed. The sample and hold technique serve as vital for converting an analog signal to a discrete signal, and it becomes much more critical when the signal is transposing hurriedly, as seen in Fig. 3b. Fig. 3c shows a close-up of the full manipulate, and Fig. 3d shows that the sample and hold is properly working since it follows the sine wave. With a matching power consumption of 0.027 and 0.23 µW, the bootstrapped S/H circuits demonstrate Signal-to-Noise and Distortion Ratio (SNDR) values of 52.95 decibels (dB) at a sampling rate of 100 mega-samples per second (MS/s) and 51.22 dB at a sampling rate of 500 MS/s for input signal frequencies 1 MHz and 10 MHz's. It also shows the voltage measured at the output of the upgraded low-power bootstrapped S/H circuit. In Fig. 4, the Fast Fourier transform (FFT) represents the sampled output voltage of the newly built low-power bootstrapped S/H circuit. The SFDR value for the circuit is indicated in FFT Fig. 4, 5, and 6. This circuit was meant to consume less power. The sampled output voltage and the spectral structure in the FFT are consistent with one another across all of the other bootstrapped S/H circuits that have been presented in Fig. 5 and Fig. 6. Fig. 5 displays the spectrum at 100 MS/s, and Fig. 6 shows the spectrum at 500 MS/s and illustrates the difference between the three variables in terms of MS/s. The key differences between the figures are outlined in Table 1. This table provides an enumeration of the many different bootstrapped S/H circuits that make use of a transmission gate as the switching element. As a consequence of this, the enhanced low-power bootstrapped S/H circuit that was developed to achieve the lowest power consumption in contrast to the others, without significantly sacrificing the Signal-to-Noise and Distortion Ratio (SNDR) performance at low and high frequencies.

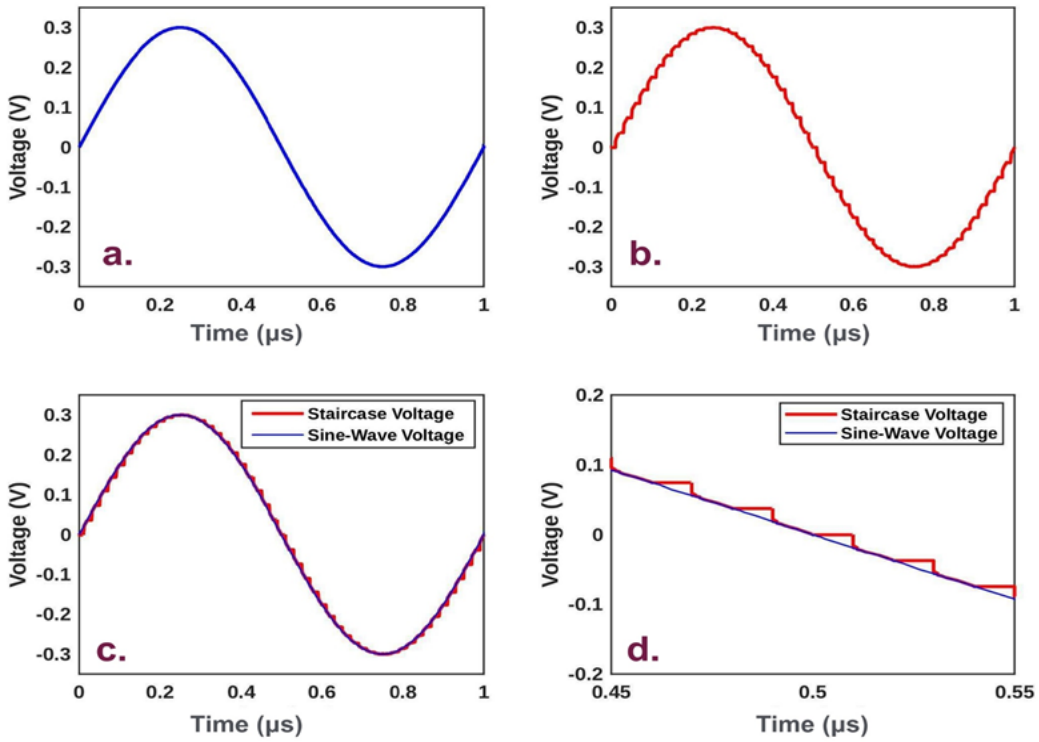

Fig. 2 *(a-d) The improved low-power bootstrapped sample-and-hold circuit's output voltage for 50MS/s*

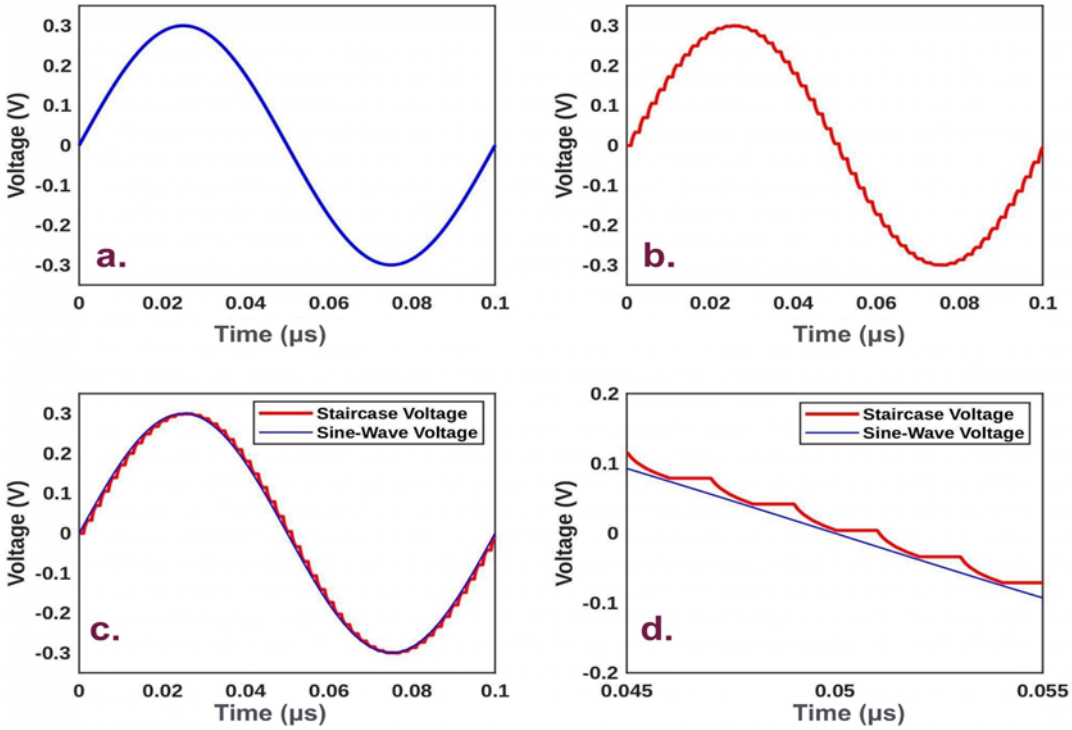

Fig. 3 *(a-d) Simulation result of sample and holding circuit of 500MS/s*

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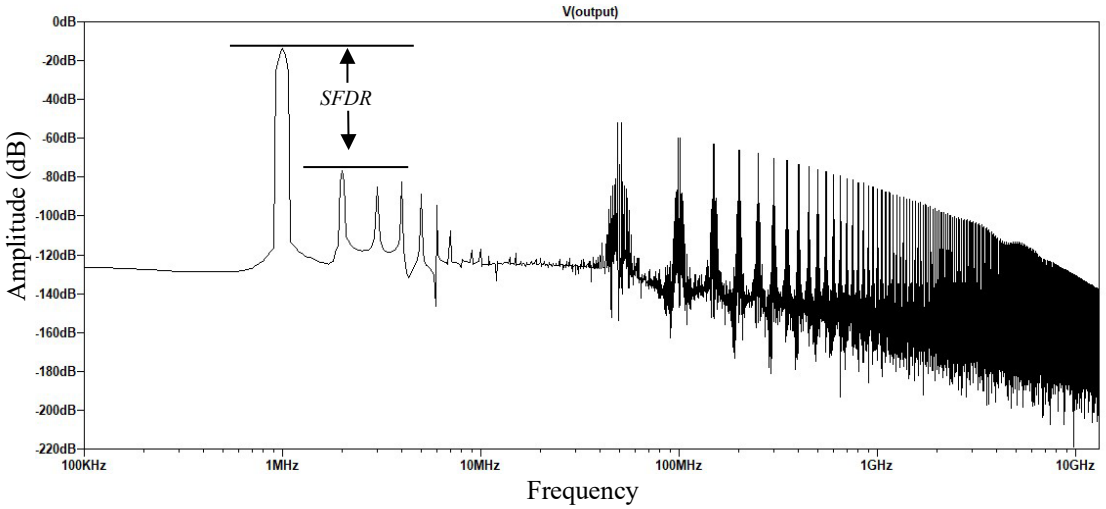

Fig. 4 *FFT spectrum of proposed low power bootstrapped circuit of 50MS/s*

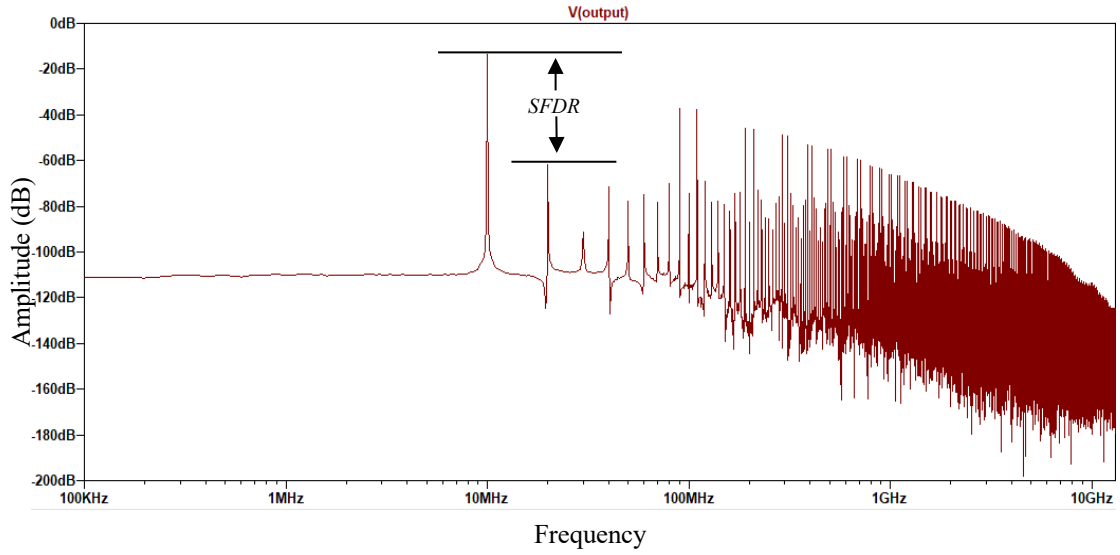

Fig. 5 *FFT spectrum of proposed low power bootstrapped circuit of 100MS/s*

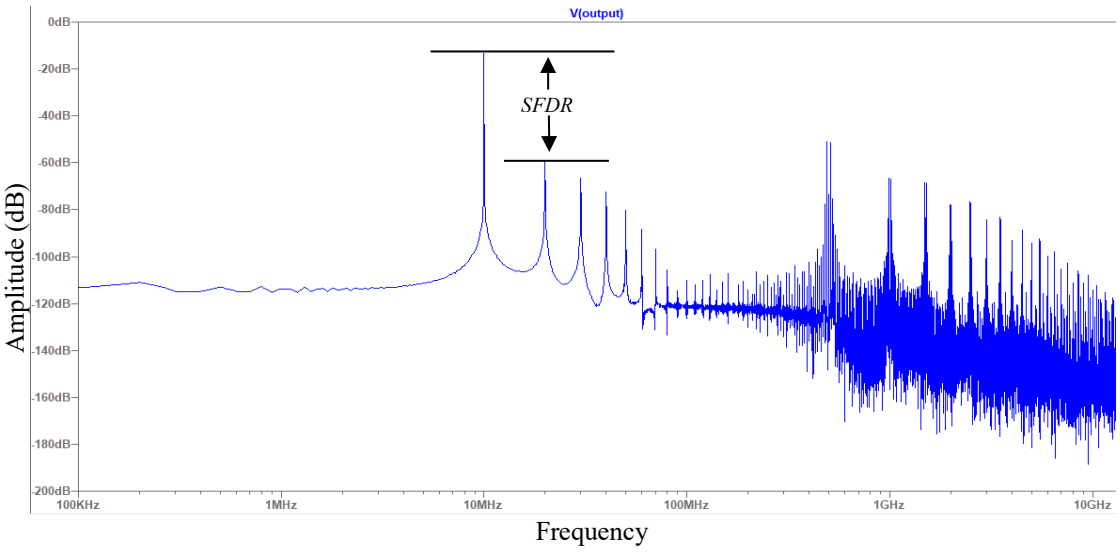

Fig. 6 *FFT spectrum for a 500MS/s proposed low power bootstrapped circuit*

5. Comparative Analysis

Table 1 tabulated a summary of simulation outcomes.

Table 1 *Summary of simulation outcomes for the proposed circuit of 50, 100, and 500MS/s*

Parameters	Proposed work 1	Proposed work 2	Proposed work 3
Technology	45nm, CMOS	45nm, CMOS	45nm, CMOS
Supply Voltage	1 V	1 V	1 V
Sampling Rate	50MS/s	100MS/s	500MS/s
Input Range	0.3 V	0.3 V	0.3 V
SNR dB	72.43	66.79	77.57
SNDR dB	52.47	52.95	51.22
SFDR dB	63.74	68.33	46.43
Power Consumption (μW)	0.21	0.027	0.23

In Table 1, the sample and hold circuit operate at a minimum supply voltage requirement of 1V; just one other device operates within this voltage range. Utilizing the most advanced technology now accessible, this study produces the tiniest sample and circuit in its particular category, with an input voltage of 0.3V, thanks to its 45 nm size. The performance is evaluated based on different sample rates just as 50MS/s, 100MS/s, and 500MS/s. Power consumption is a matter of concern in this study where the lowest number is 0.027μW at 100MS/s. On the other hand, at 50MS/s and 500MS/s the circuit consumes 0.21μW and 0.23μW respectively. Signal processing parameters are equally important, the system serves communication systems mostly. Regarding SNR, the highest sample rate applied on the circuit gives the best outcome having 77.57dB while 72.43dB and 66.79dB are observed when it operates at 50MS/s and 100MS/s. Unlike SNR, the SNDR is spotted as very stable for all the given sample rates ranging between 51dB to 53dB. SFDR is identified from the FFT analysis, and at 500MS/s, the SFDR is significantly low resulting in 46.43dB. In contrast, the circuit outputs 63.74dB at 50MS/s and 68.79dB at 100MS/s at lower sample rates. The S/H circuit consumes the least amount of power and operates at the lowest voltage feasible. Applications requiring quick data processing and stringent signal clarity requirements are a good fit for this architecture. Modern technology is combined with fast sampling speed, a broad input range, remarkable performance metrics, and energy economy in the 45nm CMOS sample and hold circuit shown in Table 1. For situations where accuracy and velocity are critical, this designates it as a robust choice. Table 2 represents the comparison between proposed work 1-3 and different research works.

Table 2 *Comparison table between proposed and other research works*

Parameters	[24]	[14]	[25]	[23]	Proposed Work-1	Proposed work-2	Proposed Work-3
Supply Voltage (V)	1.8	1	0.9	1.8	1	1	1
Technology (nm)	180	90	180	180	45	45	45
Sampling Rate (MS/s)	1	40	0.2	200	50	100	500
Input Range (V)	1.8	0.5	0.9	1.8	0.3	0.3	0.3
SNR (dB)	-	-	-	65.4	72.43	66.79	77.57
SNDR (dB)	86.94	56.7	47.4	64.9	52.47	52.95	51.22
SFDR (dB)	87.82	-	-	77.6	63.74	68.33	46.43
Power Consumption (μW)	120	20	250	6250	0.21	0.027	0.23

From Table 2 the comparative parameters used in this table are supply voltage, CMOS technology (nm), sampling rate (MS/s), input range (V), signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR), and power consumption. The three proposed works use supply voltage (1V), input range voltage (0.3V), 45nm technology and different sampling rate (50, 100, and 500 MS/s), respectively. In contrast, [21], [14], [22], and [2] employ varied supply voltages (1.8, 1, 0.9, and 1.8 V), input range voltage (1.8,

0.5, 0.8 and 1.8 V), technologies (90 and 180 nm), and sampling rates (1, 40, 0.2, and 200 MS/s), respectively. The proposed work-3 achieves a higher SNR which is 77.57 dB, whereas the other values for SNR are 65.4 dB [2], 72.43 dB (proposed work-1), and 66.79 dB (proposed work-2), respectively. Among the three proposed works, the SNDR of the proposed work-3 demonstrates better results which is 51.22 dB for 500 MS/s and 45 nm CMOS technology, whereas [22] has an SNDR of 47.4 dB for 0.2 MS/s and 180 nm CMOS technology. The proposed works 1, 2, and 3 have SFDR of 63.74, 68.33, and 46.43 dB, accordingly. In addition, [21] and [2] indicate SFDR of 87.82 and 77.6 dB, respectively. However, proposed work-2 consumes the least amount of power, measuring 0.027 µW. Additionally, proposed work-1 (0.21µW) and proposed work-3 (0.23 µW) have also lower values than others research works shown in the Table 2.

The work presented includes a 45nm CMOS sample and hold circuit that performs better than any of the four reference publications. The circuit provides 50 MS/s, 100 MS/s, and 500 MS/s sampling rates. Compared to the higher supply voltages utilized in the majority of reference papers, it can operate consistently at 1V, meaning that it can handle lesser power requirements. The proposed work uses cutting-edge 45nm technology to create circuits that are more efficient and compact than references that use 90nm or 180nm technology. The 50 MS/s, 100 MS/s, and 500 MS/s sample rates that are offered surpass the majority of other possibilities, especially those that are limited to 1 MS/s. This work can be easily adjusted to different signal amplitudes due to its remarkable input range flexibility, which spans from 0.1V to 0.3V. In terms of Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SNDR), and Spurious-Free Dynamic Range (SFDR), the presented research consistently achieves competitive values across all three sample rates, significantly surpassing the values documented in reference papers. In sharp contrast to the significantly higher power consumption seen in other reference papers, such as 6250 µW, the suggested study shows an amazing accomplishment by sustaining a power consumption of only 0.21 µW, 0.027 µW, and 0.23 µW for the difference input value. In summary, the presented work is superior to the four referenced publications because it uses less power, has more advanced technology, variable sampling rates, a wider input range, and better performance metrics. In order to further enhance performance and scalability, future developments can involve silicon implementation, integration with ADC's and adaptation for modern CMOS technologies.

6. Conclusion

A novel approach to enhancing the efficiency of S/H circuits in low and high-frequency systems is presented in this work. The research indicates a significant decrease in power consumption (0.027 µW) without compromising the 52.95dB signal-to-noise and distortion ratio (SNDR) when a tailored low-power bootstrapped S/H circuit is used. The PMOS transistor, which is used in place of the conventional multiplier circuit to provide a constant gate-source voltage for the sampling transistor, is the circuit's creative centerpiece. Using transmission gate-based sample transistors also aids in preventing the SNDR from deteriorating. This explains when compared to the other papers, the results of this work are better. For low sample frequency, the SNR is 72.43 dB, and for high sample frequency, it is 77.57 dB. According to the same SNDR, the low sample frequency is 52.47 dB, while the high sample frequency is 51.22 dB. All the experimental data in the simulations demonstrated favorable results. The proposed circuit's improved performance over earlier attempts illustrates that it can be used to create high-performance, low-power electronic devices. In conclusion, the proposed low-power bootstrapped S/H circuit is perfect for use in wireless communication systems, Internet of Things (IoT) sensors, and portable medical devices where power efficiency is crucial.

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***Conceptualization of this study and Methodology:*** *Md Hasan Maruf, Siful Islam Pranto;* ***Software:*** *Md Hasan Maruf, Siful Islam Pranto, Md. Shakib Ibne Ashrafi;* ***Data curation and writing - Original draft preparation:*** *Md Hasan Maruf, Siful Islam Pranto, Md. Shakib Ibne Ashrafi, Sadi Mohammad Moin, Mohi Uddin Ahmed, Murad Kabir Nipun, ASM Shihavuddin. All authors reviewed the results and approved the final version of the manuscript.*

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