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Modelling SOI PIN Diode for Energy Harvesting Application

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Abstract: A photodiode model which able to harvest energy in standard PIN photodiode design processes is presented, output current of most photodiodes in an open circuit is low and worsening parasitic diode effect. The purpose using this photodiode design to evaluate current and voltage performance. The photodiode was designed and simulated in COMSOL Multiphysics by using silicon material with varying thickness. High current output, wider intrinsic layer, value of breakdown voltage was achieved through varying the thickness. This photodiode current output is 9μA when the thickness is 1μm and percentage of current increment is between 6% and 18%. Width of intrinsic layer increase by 10% and breakdown voltage also increase in proportion with the width of intrinsic layer. Finally, from the studies, the current, width of intrinsic layer and breakdown voltage increase when the thickness of the model increase.

Keywords: SOI PIN Diode, Energy Harvesting, COMSOL Multiphysics

1. Introduction

Harvesting energy from the sun and other light sources is intriguing since these forms are abundant and have high energy densities when compared toward other environmental forms of energy [1]. A photodiode is a semiconductor device that uses a P-N junction to convert photons (or light) to electrical current. While the N layer does have a numerous of electrons, the P layer does have a numerous of holes. Photodiodes are frequently utilized to make devices that can efficiently detect light energy because of their great sensitivity to light [2]. Photodiodes have undergone several adjustments to increase the performance of these devices. Since its small junction region and photocurrent. Silicon photodiodes, which are composed of silicon crystals, are commonly used to detect weak signals.

The usage of a silicon-on-insulator (SOI) PIN diode in energy harvesting applications can bring several benefits compared to traditional PIN diodes. Improved performance of SOI PIN diodes has a thin silicon layer, which allows for faster switching speeds and lower capacitance compared to traditional PIN diodes. This can result in improved energy conversion efficiency for energy harvesting applications. Furthermore, it reduced leakage current the insulating layer in SOI PIN diodes helps to

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reduce the leakage current, which can result in a lower power consumption for energy harvesting systems.

Moreover, most photodiode open circuit voltage output is low. Average photodiode current produced is between 395µA to 3mA depending on illumination conditions [3]. To charge batteries or power up the sensor's circuitry, more current are needed. Additionally, thickness of the intrinsic layer affects the electric field strength within the diode and the concentration of carriers in the intrinsic region in energy harvesting. Energy conversion efficiency also shows a significant role in the success of energy harvesting using photodiodes. Percentage of energy conversion is still low. Common conversion efficiency is between 6% to 40% [4]. Energy conversion efficiency is low because of parasitic substrates from photodiodes. Through this investigation the value of output current would like to increase the value of the output current. Finally, this research is to design a PIN photodiode for an energy harvesting and to evaluate current and voltage performance of photodiodes for energy harvesting application. Figure 1 shows overall flow of the process involve in modelling SOI PIN diode using COMSOL software.

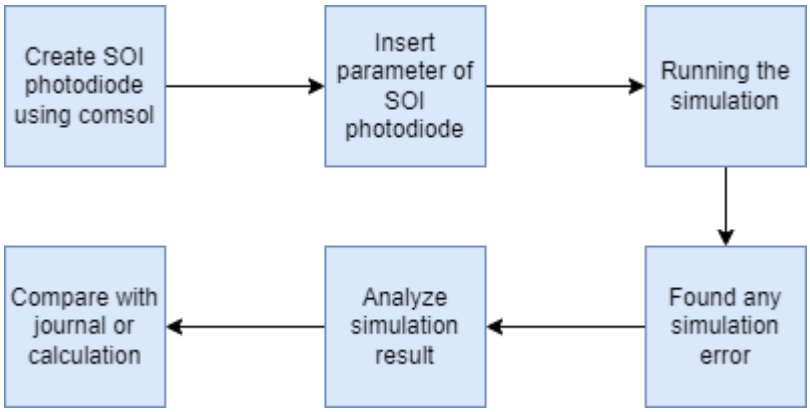

Figure 1: Process flow in Modelling PIN photodiode

1.1 Structure of PIN photodiode

Figure 2 shows the PIN diode, which is one of the most widely used photodetectors [5] because the intrinsic depletion zone can be altered to enhance the quantum efficiency and frequency response, is a special instance of a PN junction photodiode. A PN junction and an intrinsic (I) region with an inherent length make up the PIN diode.

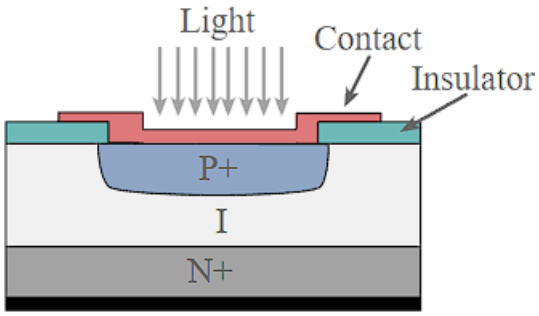

Figure 2: Structure of PIN photodiode

1.2 Thickness

Regarding improved device performance, silicon thickness or device thickness should be kept as minimal as possible. This is because as the device progresses, the control over the gate becomes less effective. It's also crucial to know what the most excellent substrate thickness to use. Results of calculating the electric field for various thicknesses. As that the thickness grows, so does the threshold voltage.

2. Methodology

The modelling of SOI PIN diode for energy harvesting application is done using Comsol Multiphysics Software. A silicon PIN diode is a type of diode that utilizes a silicon semiconductor material for the intrinsic (I) layer. P-type, intrinsic, and N-type semiconductor layers are denoted by the designation "PIN" in diodes. Current output should be higher than 3µm. Intrinsic layer must be wider to handle the breakdown voltage. Figure 3 shows the SOI PIN diode model in Comsol Multiphysics. This photodiode uses 5µm for width, 1µm for thickness for initial simulation and changes the thickness after that. The negative contact is typically connected to the N-type region, and the positive contact is attached to the P-type region. Applying 2V at the negative contact in a PIN diode will result in a reverse bias condition.

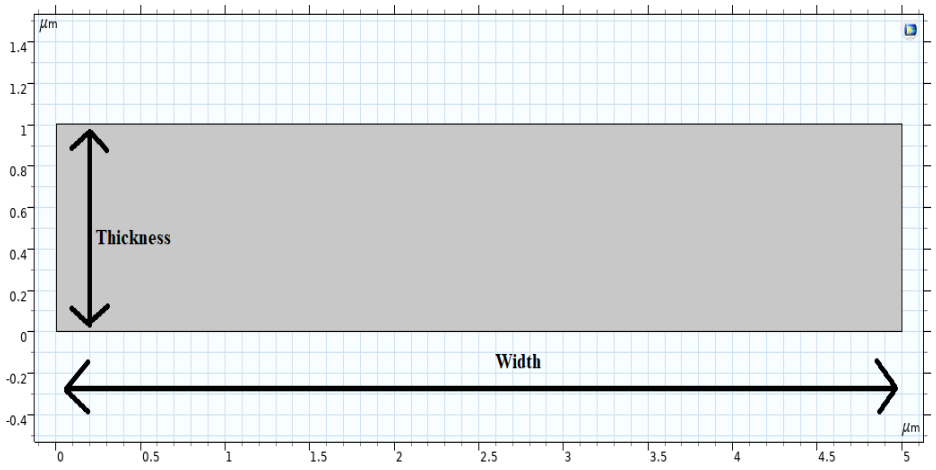

Figure 3: Structure of PIN photodiode

The wavelength value used in the design is 870 nm because the wavelength range of silicon to operate is between 400 nm until 1000 nm. Table 1 shows the refractive index of silicon is 3.9766. The spontaneous emission lifespan is the length of time it takes for an emission to decay on average. This spontaneous decay happens on average in a millisecond for some stimulated energy levels, including (2×10^{-9}). In the semiconductor is a measure of its transparency to incident spectral radiation. (1×10^{6}) out-of-plane thickness is set for this modelling. Out of plane thickness is the length of the object that Comsol assumes in this modelling. Finally, Incident power for out-of-plane thickness is set for 1.05 Watt. Incident power is a power that been use to diode as a input voltage to make the diode function.

Table 1: Parameter used in modelling SOI PIN diode

Name	Description	Value
w_dom	Width	5µm
h_dom	Thickness	1µm
V_n	n-contact voltage	2V
V_p	p-contact voltage	0V
n0	Refractive index of Silicon	3.9766
Pin	Incident power for out-of-plane thickness	1 x 10^{-5}

Wavelength sweep and frequency stationary are the equations and formulas used in the semiconductor component of Comsol, where eq. 2 E (g,0) is the band gap and X 0 is the electron affinity. Eq.1 where N_v is valence band and N_c is conduction band. μ_n is electron mobility and μ_p is hole mobility. Wavelength sweep is a type of parameter sweep where the wavelength of the input light is varied over a specified range while the frequency is held constant. The frequency stationary option in COMSOL means that the frequency of the input light is fixed at a specified value and the wavelength is held constant. In contrast, when the frequency is stationary, the simulation will solve the problem for a single frequency, and the results will not be plotted as a function of wavelength. Both options have different uses, wavelength sweep is useful for example when studying the behavior of a material or device as a function of wavelength, while frequency stationary is useful when studying the behavior of a material or device at a specific frequency.

$$J_n = qpu_p\nabla \mathrm{E}_v + qD_p\nabla_p - qpD_p\nabla in(N_v) + qpD_{p,th}\nabla in(T)\ \ D_p = \mu_p k_B TG\left(\frac{p}{N_v}\right) \qquad Eq.1$$

$$E_c = -(V + X_0), \qquad E_v = -\left(V + X_{0+}E_{g,0}\right) \qquad Eq.2$$

COMSOL provide user to have total control over the specification and application of your material properties using the Model Builder and Material Manager in COMSOL Multiphysics. You may handle all the materials for your model in one location with the Material Browser, that can be enhanced by the Material Library. Data about 12,763 different materials, including elements, minerals, metal alloys, thermal insulators, semiconductors, piezoelectric materials, and more, are available in the material library. Figure 4 shows the chosen material is Silicon because Silicon diode is easier to produce than other diode material due to the widespread availability of silicon. Silicon is used for modelling photodiode because of various visible-light applications in electronics, such as for a light dimmer. Silicon is also sensitive to the wavelengths of visible light and a reliable material for good current output.

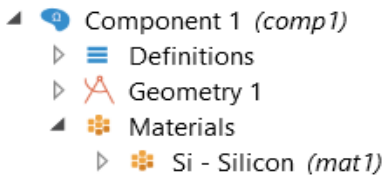

Figure 4: Silicon material in component 1

In one multiphysics file, as shown in Figure 5, various model components can be described independently. For instance, when handling some components of the overall model in 2D and others in 3D, definitions are found under the Component branch. Definitions that mention a geometry's domains, dimension, or coordinate name in some form must be kept apart in different Component branches. Comsol-defined boundary system and view are present in the defining branch. the boundary system On 2D boundaries (t, n) as well as 3D borders, a boundary system is a local base vector system (t1, t2, n). Use it to implement loads as well as other boundary conditions to a boundary that isn't in line with the overall Cartesian coordinate system in a regular or tangential direction.

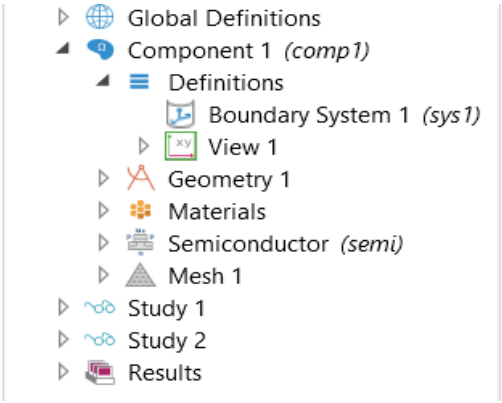

Figure 5: Definition section in Comsol

3. Results and Discussion

The photodiode model was given the necessary physical modules, boundary conditions, and recommended geometry by all models created with COMSOL software. After that, the model is meshed to produce the desired outcomes. The many equations that occur in semiconductors are resolved using Maxwell's equations, Boltzmann transport theory, and Neumann boundary conditions, which also offer boundary conditions between the various junctions. The thickness has all been varied.

3.1 Influence of different thickness

The electrical properties were shown for several thicknesses in Table 2 for modelling SOI PIN diode. The thickness of the PIN diode can affect its intrinsic width.

Table 2: Thickness and width parameter used for modelling SOI PIN diode

No	Thickness	Width
1	0.6 µm	5 µm
2	0.7 µm	5 µm
3	0.8 µm	5 µm
4	0.9 µm	5 µm
5	1 µm	5 µm

3.2 Intrinsic width and breakdown voltage

When compared to a typical PN junction diode, the PIN diode's intrinsic layer is what causes the shift in attributes. The semiconductor that is undoped or nearly undoped is found in the intrinsic region. Figure 6 shows the doping profile throughout the device when the thickness is varied. Figure 5 shows the intrinsic width (undoped) region changing between around 0.15 m and 0.85 µm depending on the respective thickness. Generally, a thinner PIN diode will have a intrinsic width, making it more suitable for high-frequency applications. On the other hand, a thicker PIN diode will have a intrinsic width, making it more suitable for low-frequency applications. It is important to note that the optimal thickness of a PIN diode will depend on its intended application and operating conditions.

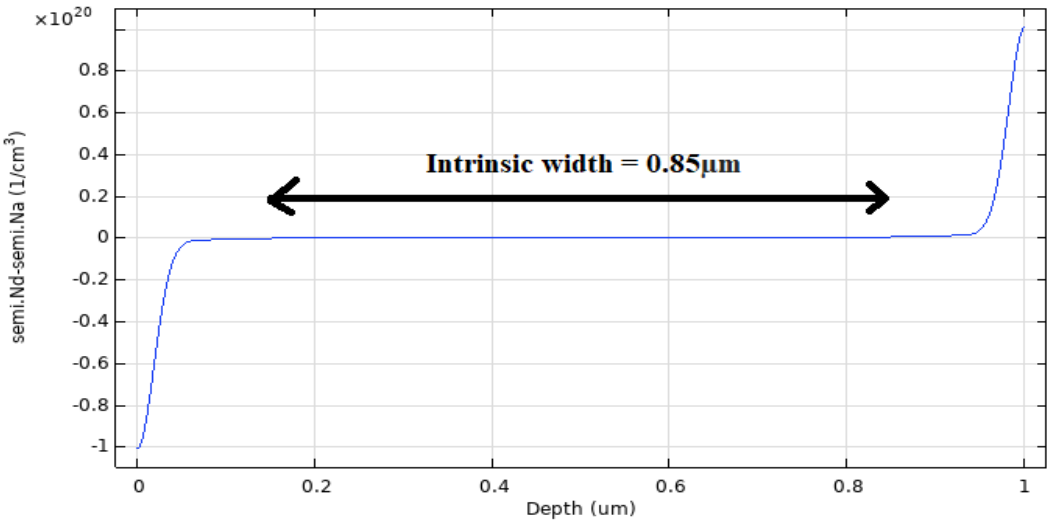

Figure 6: Intrinsic Layer Characteristic for 1µm Thickness

V_{BD} is describe as the breakdown voltage in PIN diode. To obtain parameters of E_M is through the constant value of PIN diode and W is obtained through simulation. V_{BD} for 1µm thickness is 0.255V and value drop as thickness is decrease. From eq.3 V_{BD} obtained is 0.255V, where W is 0.85µm and E_M is 3 X 10^5 for silicon. From Table 3 increase in percentage of intrinsic width is 10% when the thickness is increase. Table 3 shows breakdown voltage result from calculation according to the equation in 4. Based on the Table 3 show percentage of breakdown voltage increase when the intrinsic width is increase is between 10% to 18% for during all simulation. The breakdown voltage of a PIN diode is related to the electric field at the P-N junction. Increasing the thickness of the intrinsic (I) layer of a PIN diode will increase its breakdown voltage, making it more suitable for high-power applications.

Table 3: Intrinsic width and breakdown voltage based on thickness

No	Thickness	Intrinsic Width	Breakdown Voltage
1	0.6 µm	0.5 µm	0.15V
2	0.7 µm	0.55 µm	0.165V
3	0.8 µm	0.65 µm	0.195V
4	0.9 µm	0.75 µm	0.225V
5	1 µm	0.85 µm	0.255V

$$V_{BD} = E_m W \qquad eq.3$$

Where V_{BD} = Breakdown voltage, E_M= Electric field, W = Intrinsic width

3.3 Current Characteristic

Figure 7 shows the plot of the current through all the thicknesses of the photodiode that varied as a function of the incident photon wavelength. Since the longest wavelength has energy under the band gap and shouldn't be absorbed, there is not much current at the long wavelength end of the sweep. The current curve of the model states that the ratio of incident photons to absorption probabilities determines the rate of photon absorption.

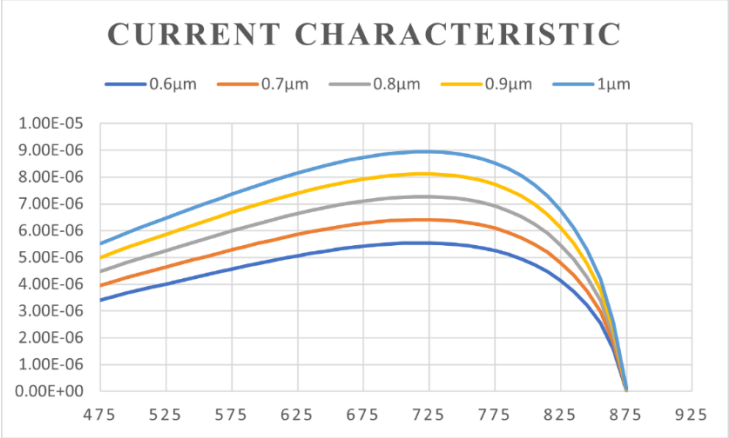

Figure 7: Current characteristic for different thickness

As shown in Table 4, as the thickness is reduced, the photon energy is subsequently elevated, and the current gradually declines as the photon energy is further increased. The current rapidly climbs to a peak value of 0.09 A at thickness 1 um. Based on the Table 4 show percentage of current increase when the diode thickness is increase is between 6% to 18% during all simulation. The thickness of a PIN diode can affect its current output, but it depends on the specific application and operating conditions. In general, a thicker PIN diode will have a higher doping concentration and a lower resistance, which can lead to a higher current output. On the other hand, a thinner PIN diode will have a lower doping concentration and a higher resistance, which can result in a lower current output. The optimal thickness of a PIN diode for a particular application will depend on the desired current output, as well as other factors such as the reverse voltage and the frequency of operation.

Table 4: Current output according to respective thickness

No	Thickness	Current output
1	0.6 µm	0.55 mA
2	0.7 µm	0.65 mA
3	0.8 µm	0.75 mA
4	0.9 µm	0.8 mA
5	1 µm	0.9 mA

4. Conclusion

The proposed PIN photodiode is constructed effectively using Comsol software, and the simulation results also achieve the preferred value that shown in Table 5. The maximum current output for the result simulation is 0.09 mA, Intrinsic layer width also increase in 10% increment when thickness of model increase. Breakdown voltage is increase 10% to 18% according to the increasing if intrinsic layer width during all simulation. The SOI PIN diode simulation output has followed the theory of PIN diode.

Table 5: Simulation output according to respective thickness

No	Thickness	Current output	Breakdown voltage	Width Intrinsic layer
1	0.6 µm	0.55 mA	0.15V	0.5 µm
2	0.7 µm	0.65 mA	0.165V	0.55 µm
3	0.8 µm	0.75 mA	0.195V	0.65 µm
4	0.9 µm	0.8 mA	0.225V	0.75 µm
5	1 µm	0.9 mA	0.255V	0.85 µm

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