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Design and THD Analysis of 5-Level Cascaded Multilevel Inverter

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Abstract: One of the electronic equipment that gives researchers concern for the enhancement of generating a neat power source is an inverter, which can be defined as a device or electric circuit that converts direct current (DC) to alternating current (AC). As part of this project, a model of a multilevel inverter that uses a 5-level cascaded H-bridge of a multilevel DC-AC inverter is going to be developed which will reduce the total harmonic distortion (THD). In this experiment, the total harmonic value of a traditional 3-level multilevel inverter is compared with the outcome of a 5-level multilevel inverter. In particular, the utilisation of a cascaded H-Bridge architecture in conjunction with a sinusoidal pulse width modulation (SPWM) result in a greater output power with a multilevel configuration. The experimental result that has been included demonstrates how effective the inverter that has been proposed is. As a result, the goal of this project is to analyse and get the lower amount of THD. This project has obtained the voltage output waveform of a 5-level inverter hardware circuit and its THD% which will be covered in output parts.

Keywords: Cascaded H-Bridge Multilevel Inverter, Voltage THD, SPWM

1. Introduction

For a few reasons, multilevel inverters have replaced normal inverters, thanks to the development of inverters. High voltage application, low electromagnetic interference, lower voltage strains on electronics and low total harmonic distortion (THD) are just some advantages of multilevel inverters [1]. Most often used inverter topologies are a diode-clamped converter (DCC), a flying-capacitor converter (FCC), and a cascaded multilevel inverter (CMI).

The modular structure of CMI sets it apart from the other two topologies, making it easy to design, synthesise, and repair [2]. Through clamping diodes, DCC raises the voltage levels. As a means of adjusting the voltage, the capacitors are linked together in series. This is a significant issue for electronic devices. Voltage balancing is more difficult in FCC because of the increased number of clamping capacitors. Hence, the DCC and FCC are not used for this project [3]. CMI has many benefits, such as

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high-power quality, which lets motors work better, and low THD, which reduces the need for output filters [4]. It also has a low switching frequency, which reduces switching losses, and high modularity, which lowers costs and improves reliability [5].

CMIs use several DC power sources. The output of each inverter is different depending on its level. The voltage levels of all the cells are added together to produce the output voltage. The 2n+1 is the output voltage's number of levels. The 'n' represents the number of inputs [6].

2. Methodology

This section will demonstrate the overall approach taken to complete this project. It includes a number of essential parts that must be present in order to accomplish the objectives of the project. The goal of this project is to simulate PWM signal for a 5-level and 3-level cascaded multilevel inverter circuit using MATLAB/Simulink and analyse its THD of voltage output. MATLAB/Simulink software is used to obtain the result of simulation. The hardware of circuit of 5-level cascaded multilevel inverter is presented at the end of this project.

2.1 Project Flowchart

The research framework for this project is presented in Figure 1. It will start with a review of the literature and the collection. Following the project execution planning, design a 5-level and 3-level cascaded multilevel inverter using MATLAB/Simulink software and run the circuit simulation. This procedure will be repeated until the output of the voltage waveform and the THD result is acceptable. Following the simulation, the hardware circuit will be designed. An oscilloscope will then be used to examine the output voltage waveform and THD values. This process will be continued until the output of the voltage waveform and the THD result is acceptable. The desired output will then be compared and analysed between the simulation software and the hardware simulation for 5-level cascaded multilevel inverter.

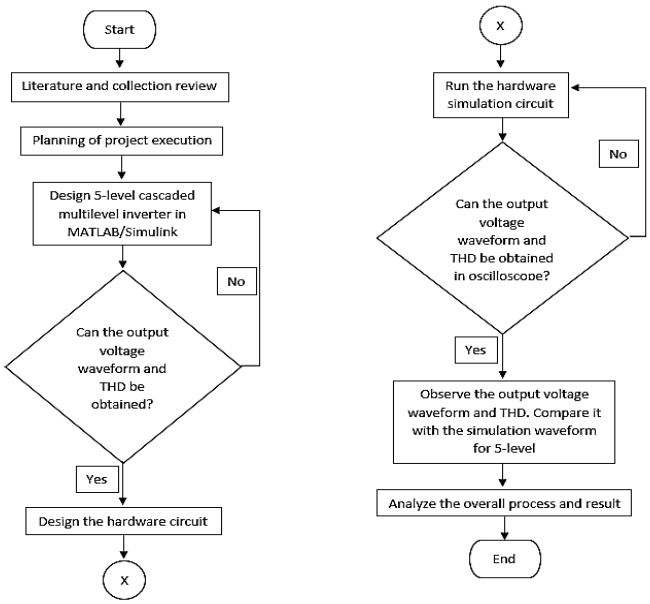


Figure 1: Flowchart of this project

2.2 Block Diagram of Multilevel Inverter

Figure 2 illustrates the block diagrams of Simulink designed 5-level multilevel inverters. The block diagram of 5-level uses 8 MOSFET for its block diagram.

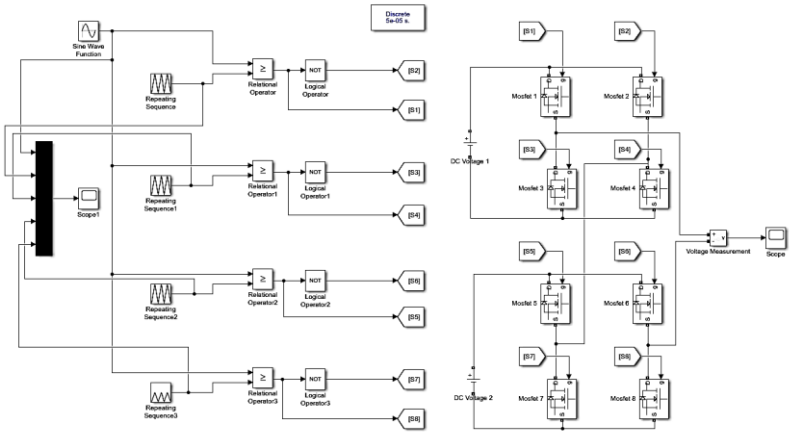


Figure 2: MATLAB/Simulink block diagram of 5-level multilevel inverter

For better understanding, Table 1 has been created in order to make it easy to read the switching state. As per table, there are 5 operating modes of 5-level circuit which are 2Vdc, Vdc, 0, -Vdc and -2Vdc.

Table 1: Switching State of 5-level circuit

Voltage (Vo)	S1	S2	S3	S4	S5	S6	S7	S8
2Vdc	1	0	0	1	1	0	0	1
Vdc	1	0	0	1	0	0	1	1
0	0	0	1	1	0	0	1	1
-Vdc	0	1	1	0	0	0	1	1
-2Vdc	0	1	1	0	0	1	1	0

2.3 Simulation using Proteus 8 Professional

Figure 3 illustrates the schematic diagram of a simulation circuit of a 5-level multilevel inverter using Proteus 8 software. The circuit was connected to an Arduino Uno which has been put coding inside it and also an oscilloscope which functions to display the output waveform.

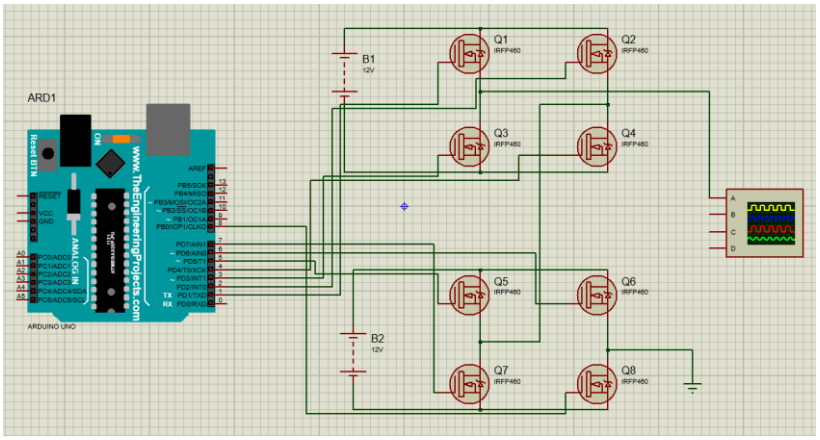


Figure 3: Schematic Diagram of Simulation in Proteus 8 Software

3. Results and Discussion

This section compares and contrasts the 5-level and 3-level cascaded H-bridge multilevel inverters via the perspective of modelling the outcomes and analysing total harmonic distortion (THD). This section also presents the Simulink block diagram for the mathematical model of a multilevel inverter system and the hardware output result. The comparison table of the hardware and simulation are stated at the end of result parts.

3.1 Output Voltage Waveform of Simulation in MATLAB/Simulink

Multilevel inverter output voltage waveforms are shown in Figures 4 and 5. Since the 5-levels have two voltage supplies of 12Vpeak each, they have an output voltage of 24Vpeak instead of the 3-levels output voltage value of 12Vpeak, which have the same 12V supply. In MATLAB/Simulink, the voltage measured is in Vpeak meanwhile in oscilloscope it will be measured in Vrms which results in a difference value which actually is the same if it be converted to one another.

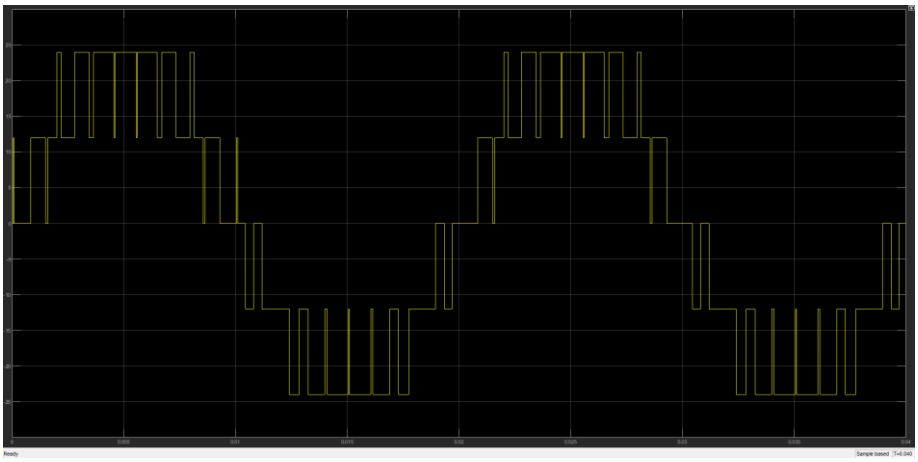


Figure 4: Output Voltage of 5-Level Multilevel Inverter

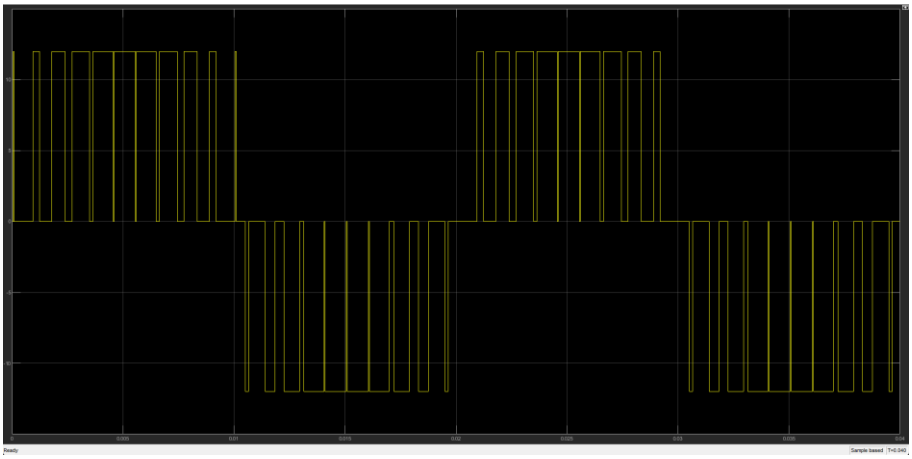
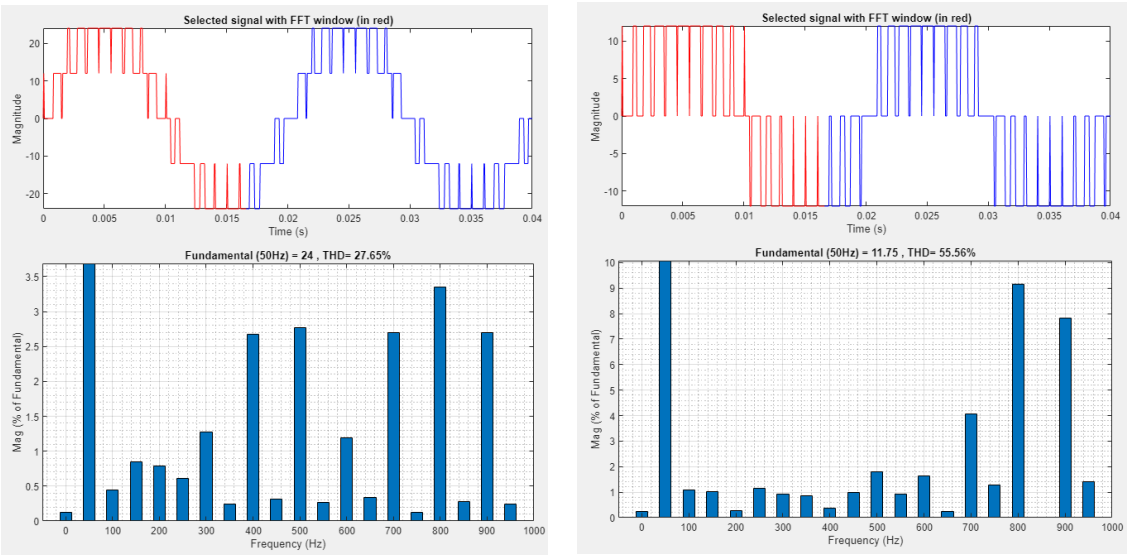


Figure 5: Output Voltage of 3-Level Multilevel Inverter

3.3 Total Harmonic Distortion using FFT Analysis in MATLAB/Simulink

Figures 6(a) and 6(b) display a THD comparison of 5-level and 3-level cascaded H-bridge multilevel inverters. It can be concluded that the 5-levels have much lower THD with value 27.65% than 3-levels with value of 55.56%. A greater reduction in THD% can be achieved by increasing the number of levels, as the THD% decreases with increasing level.



(a) **(b)**

Figure 6: THD of Multilevel Inverter (a) 5-level (b) 3-level

3.4 Lab Setup of Overall Circuit

Figure 7 shows the setup that has been done in the laboratory. The equipment used is a digital oscilloscope which functioned to produce the output voltage waveform and the DC power supply functioned to give 12V at both of the input 1 and 2. The Arduino is connected to the gate driver which will give the PWM pulses for each MOSFET meanwhile the gate driver circuit will be connected to the Arduino, 8 pieces of 9V battery, all MOSFET gate pins and source pins. The laptop was used to supply the Arduino. The voltage output waveform will then be displayed on an oscilloscope after the output has been connected to the instrument.

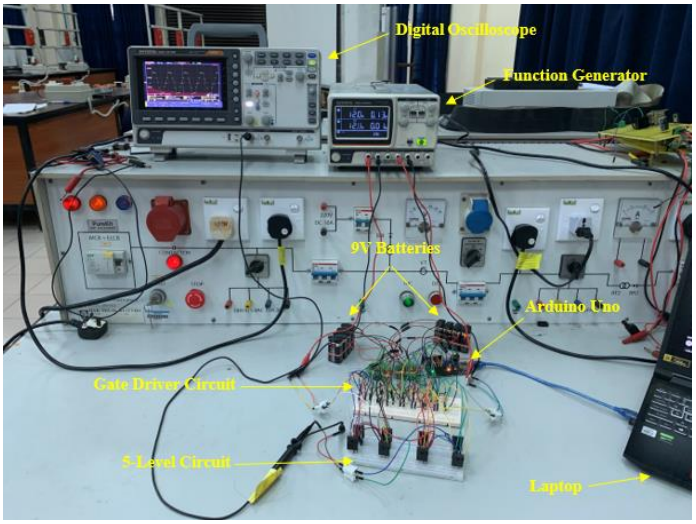


Figure 7: Overall Setup Equipment in Laboratory

3.5 Output Voltage Waveform of Hardware Circuit

Multilevel inverter output voltage waveforms that have been obtained through an oscilloscope are shown in Figure 8. Since the 5-levels have two voltage supplies of 12Veak each, they have an output voltage of 24Vpeak should be present. The output of a hardware 5-level multilevel inverter obtained is 16.5Vrms and by using the formula of Vrms=Vpeak × 0.707.

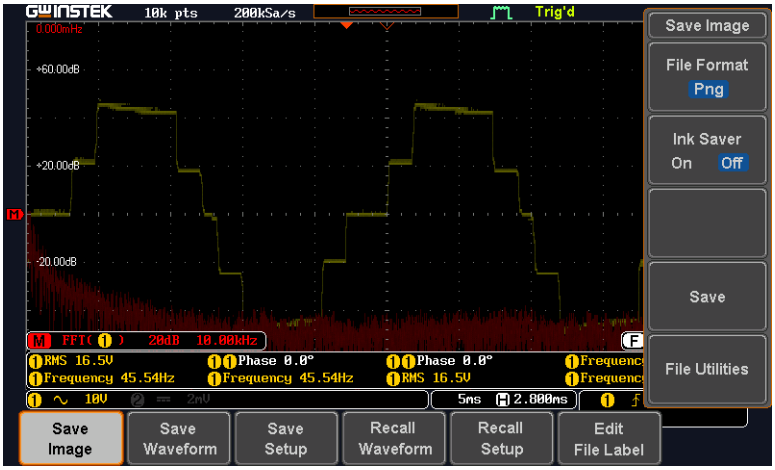


Figure 8: Hardware Output Voltage of 5-Level Multilevel Inverter

3.6 FFT of Voltage Output Waveform of Hardware Circuit

Figure 9 depicts the FFT for 5 level cascaded H-bridge multilevel inverters. The FFT graph will be used to obtain the THD% which the data of FFT in Microsoft Excel will be converted into THD% by using the existing formula. This FFT is obtained by saving the files of the waveform in an oscilloscope using pendrive.

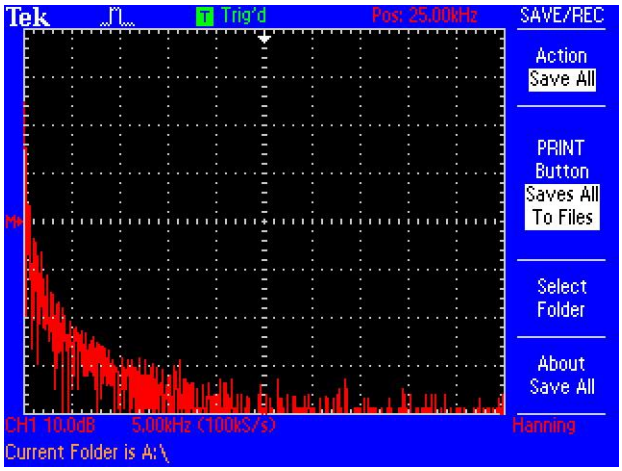


Figure 9: FFT Graph of Hardware Output 5-Level Multilevel Inverter

3.6 THD% Comparison between Simulation and Hardware Output Result

As shown in Table 2, the simulation value of THD% of 5 levels inverter is 27.65 meanwhile the value of hardware THD% is 21.08 after being calculated using Microsoft Excel which resulted in a difference of 6.48. The THD% of hardware appears to be lower and better than simulation. The output voltage between simulation and hardware is almost the same with only 0.47 voltage difference. A step-up transformer with a turning ratio of will be used to boost the circuit's voltage.

Table 2: Comparison of Simulation and Hardware THD%

Parameter	Simulation	Hardware
THD%	27.56	21.08
Output Voltage (Vrms)	16.96	16.50

4. Conclusion

Two normal full H-bridges are used to propose a 5-level CHB Multilevel Inverter. The CHB Multilevel Inverter can be built with a ready component that is often used instead of a component that the user requests. In fact, compared to the other two topologies, diode clamp and flying clamp capacitors, the cascaded H-bridge topology needs less parts, which is a big plus. The inverter was able to achieve higher performance output voltage and current despite requiring a large number of components to generate output at a higher level. System total harmonic distortion (THD) is greatly decreased, resulting in enhanced system performance. When compared to a standard inverter, the THD obtained at the output from a multilevel inverter with five levels and three levels is superior. In conclusion, the 5-level (CHB) Multilevel Inverter simulation model was successfully simulated in MATLAB Simulink utilising the SPWM approach. The results of a comparative examination of THD and output voltage over simulation and hardware are obtained and analysed. Finally, this 5-level (CHB) Multilevel Inverter can be used to reduce the THD% and replace the conventional inverter that is being used.

Acknowledgement

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