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VLSI Design for Home Automation System

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Abstract: The home automation system is designed to enhance the comfort, convenience, and security of a household by integrating various subsystems such as lighting control, temperature regulation and security monitoring. The proposed solution involves integrating a security system, lighting system, HVAC system and water tank system into Very Large-Scale Integration (VLSI) technology. The design was optimized for area and timing using the 32 nm Complementary Metal-Oxide Semiconductor (CMOS) technology. The Register Transfer Level (RTL) logic design, along with its corresponding testbench, was written in Verilog Hardware Descriptive Language (HDL) code. The design underwent pre-functional verification using ModelSim-Altera and post-functional verification using Synopsys VCS. Once the design passed verification, it was converted into a gate-level netlist and underwent physical synthesis. the proposed design demonstrated successful operation by generating accurate outputs for the actuators based on the input signals from the sensors. This indicates that the design is functioning as intended. The final layout of the design was implemented with an area of 659.95 μm^2, indicating efficient use of physical resources. The total power consumption of the design was measured at 206.35 μW, reflecting optimized power usage. The design exhibited a positive timing slack of 0.46 ns, indicating that the timing requirements were comfortably met. Furthermore, the design passed the physical verifications with no reported Design Rule Check (DRC) violations or Layout Versus Schematic (LVS) violations.

Keywords: Home Automation System, VLSI, Verilog HDL

1. Introduction

The fundamental home automation system aims to cater to the host's needs and maintain a safe and comfortable environment [1]. A comprehensive home automation system can control multiple parameters simultaneously, allowing homeowners to relax without constant monitoring of windows and doors. It is estimated that the household penetration of such systems will grow from 13.8% in 2022 to 26.0% by 2027 [2]. The system's components are classified into sensors, controllers, and actuators [3]. Prior research includes a smart home using FPGA, employing Finite State Machine and Verilog HDL to control applications like fire alarms, lighting, heaters, and coolers [4]. Another proposal suggests integrating home automation and security using FPGA [5]. An automation system focused on user

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security, with features like password door locks and alarms, has also been introduced [6]. Additionally, an intelligent home model using Application Specific Integrated Circuit (ASIC) design flow was presented [7], but without performance analysis at the ASIC level. As part of the project, an advanced home automation system controller was proposed, integrating security, lighting, HVAC, and water tank systems using VLSI technology. The design considers parameters like area, timing, and dynamic power to achieve a small and compact controller.

2. Materials and Methods

The proposed design incorporates a top-level module that employs a bottom-up methodology, utilizing Verilog Hardware Descriptive Language (HDL). This module integrates door alarm, HVAC, lighting control, fire alarm and water tank level. A clock frequency of 142.86 MHz has been established for the design. Table 1 presents the design specifications for the Register Transfer Level (RTL) logic design of the four systems.

Table 1: Design specification of the home automation system controller

System	Input Sensor	Condition	Output
HVAC	PIR Sensor, 8-bit Temperature Sensor	Temperature < 16 ℃	Heater
		16℃ ≤ Temperature < 22℃	Fan with Speed 1
		22℃ ≤ Temperature < 27℃	Fan with Speed 2
		27℃ ≤ Temperature < 32℃	Fan with Speed 3
		Temperature ≥ 32 ℃	Aircon
Lighting	PIR sensor, Lux sensor	Lux ≤ 200 & Motion	Lamp On
Security	Smoke sensor	Smoke sensor =1	Fire Alarm On
	12-bit Hexadecimal Password Door Lock	Passwor Input = Saved Password	Door Unlock & Green Light
		Passwor Input ≠ Saved Password	Trial count +1 & Yellow Light
		Trial count = 3	Door Alarm & Red Light
Water Tank	7-bit Water Level Sensor	Water Level < 50 %	Water Pump On, Buzzer On
		50% ≤ Water Level < 90 %	Water Pump On, Buzzer Off
		Water Level ≥ 90%	Water Pump Off, Buzzer Off

Once the RTL logic design of each module is verified using Synopsys VCS, it is loaded into the Synopsys Design Compiler for logical synthesis, utilizing the 32 nm Complementary Metal-Oxide Semiconductor (CMOS) technology library. The design undergoes extensive area and power optimization. Subsequently, the same 32 nm CMOS technology library is used for physical synthesis using Synopsys IC Compiler. The gate-level netlist is imported into the IC Compiler, and a floorplan is created, aiming for a core utilization ratio of 0.8. Standard cells are then placed within the core area. Clock Tree Synthesis (CTS) is performed to establish the clock distribution within the design. Next, signal nets are routed, incorporating extra power optimization techniques. Before finalizing the process, the layout of the design undergoes physical verifications with no reported Design Rule Check (DRC) violations or Layout Versus Schematic (LVS) violations.

3. Results and Discussion

Based on the system's design specification in Table 1, Figure 1 demonstrates that all the actuators within the top-level module are capable of responding to their respective inputs provided by the sensors. This module allows users to initiate security verification by confirming the input password and disabling the alarm function. The top-level module operates with a clock period of 10ns, and its output waveform represents the signals generated by the module over time. By analyzing the output waveform, one can observe the behavior of the module's actuators in response to the inputs from the sensors. Each actuator's activation and deactivation can be tracked, indicating how the system's different functions are carried out.

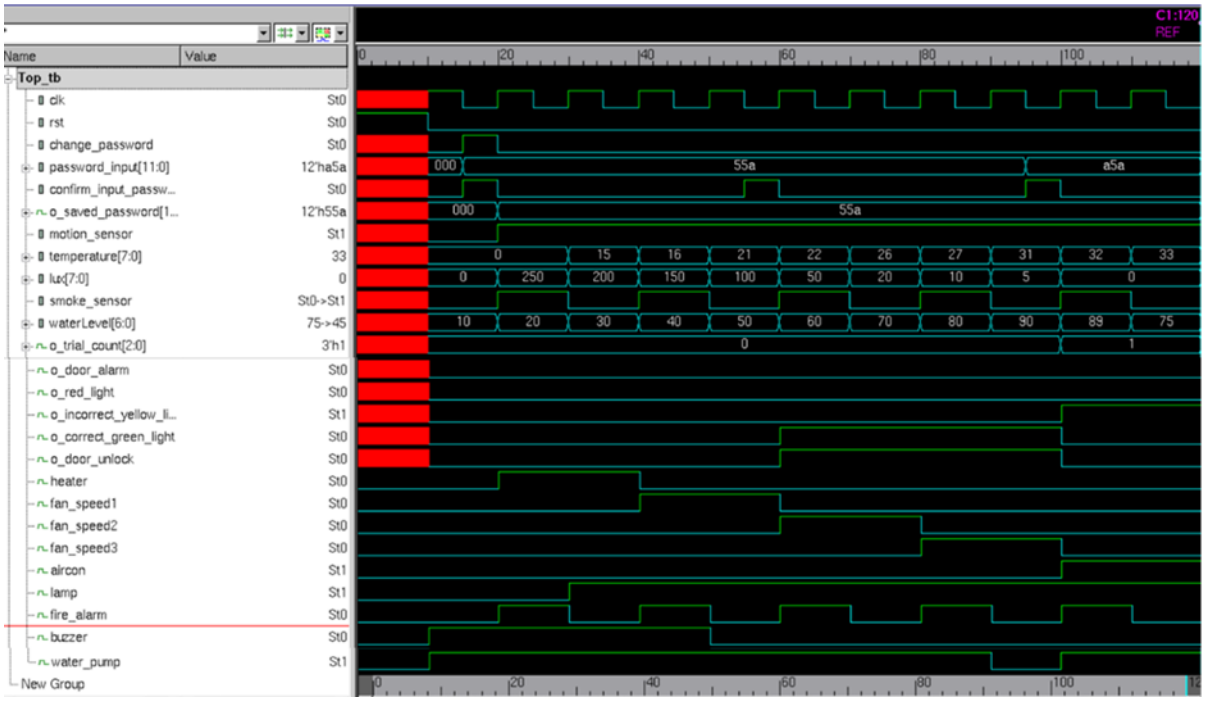

Figure 1: Output waveform of the top-level module with a 10ns clock period

The design metrics obtained during logical synthesis and physical synthesis using the same technology library are presented in Table 2. The physical synthesis phase successfully achieved lower values for both total area and timing slack for the setup check. The timing slack for the setup check in physical synthesis is 0.46 ns, which is 0.04 ns lower than the timing slack for the setup check during the logical synthesis phase. Furthermore, the physical synthesis yielded a total area of 659.95 μm^2, which is 7.31 μm^2 lower than the area obtained in the DC Compiler. Figure 3 illustrates the final layout of the design. The total power consumption of the final layout is 206.35 µW, which is 9.50 µW higher than the total power consumption during the logical synthesis phase. Figure 2 illustrates the final layout of the design.

Table 2: Summary of the performance report in logical synthesis and physical synthesis

Design Metrics	Logical Synthesis (Design Compiler)	Physical Synthesis (IC Compiler)
Timing Slack for Setup Check (ns)	0.50	0.46
Total Area (μm^2)	667.31	659.95
Total Power (µW)	196.85	206.35

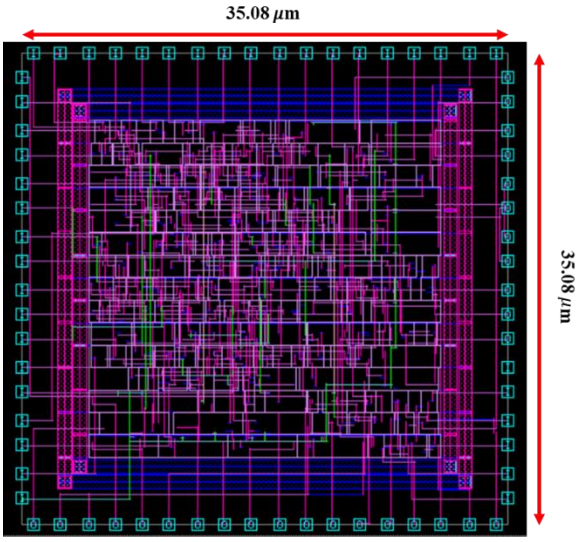

Figure 2: Final Layout of Home Automation System Controller

4. Conclusion

The project involved the successful development of a small and compact home automation system controller using VLSI technology. Each integrated system within the controller operated correctly in response to the corresponding inputs. This controller has the potential to be integrated with additional systems or peripherals, enabling the creation of more affordable and compact home controller devices. By doing so, the number of components required for the home system can be reduced. In future iterations, it is possible to incorporate more control features and voltage fluctuation detection blocks into the system, enhancing its capabilities.

Acknowledgement

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