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Smart Traffic Light Controller with Flexible Light Period

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Abstract: This article presents the development of a smart traffic light controller with a flexible light period to effectively address traffic congestion. In Malaysia, traffic congestion has become a significant problem, and conventional traffic lights with fixed light sequences and timing contribute to the issue. To mitigate this problem, a smart traffic light controller is proposed, which adjusts the light sequences at two adjacent intersections based on the current traffic congestion levels. The methodology involves designing the controller circuit using Verilog HDL, performing functional verification using ModelSim, conducting logic synthesis, and generating the layout using Synopsys for physical implementation. The functional simulation validates the correctness of the controller's outputs according to the specifications. The synthesis results demonstrate a total area of 496 µm2, total power consumption of 146 mW, and compliance with timing specifications. The results indicate that the developed traffic light controller can effectively manage traffic at intersections by dynamically adapting to the prevailing traffic congestion. The flexibility of the proposed technique allows its application to various traffic light configurations. Overall, this study contributes to the field of traffic management by offering an intelligent solution to reduce traffic congestion and improve the efficiency of traffic flow.

Keywords: Smart Traffic Light Controller, Flexible Light Period, Traffic Management

1. Introduction

Based on the traffic index by country 2023, Malaysia has ranked 21st place worldwide and 11th place in Asia which shows that traffic congestion is one of the biggest concerns in the country [1]. The prevalence of heavy traffic congestion, particularly in urban regions, is primarily attributed to the rising number of vehicles on the road [2]. According to road safety experts, 33.3 million vehicles were registered last year while the human population last year stood at 32.6 million which the vehicle population has surpassed the human population in our country [3].

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Fixed-time traffic lights are commonly seen on the roads. But fixed-time traffic lights have a lack of adaptability to traffic conditions due to their predetermined system resulting in low efficiency of traffic management [4]. The time period of the fixed-time traffic lights is predetermined. For instance, there may be instances where the green time is too short despite a significant number of vehicles waiting, while other times, the green time may be excessively long even when the road is empty due to the varying conditions at each intersection [5].

Besides, most of the intersections, especially those located in urban areas are not isolated to each other [6]. Therefore, traffic congestion can also be caused by the two adjacent intersections if their signal timings are not synchronized, leading to conflicting traffic flows. Inefficient coordination between the intersections can result in increased delays, long queues, and reduced traffic flow efficiency, ultimately contributing to congestion in the area.

In order to improve the efficiency of traffic flow management, an adaptive multi-intersection control-based smart traffic light controller is introduced in this work. An adaptive control method is a system that refers to technologies that collect the data of current traffic demand to alter the light sequences in coordinated traffic signal systems to optimize traffic flow [7]. While multi-intersection traffic light control is a traffic light system with a signal timing plan that manages more than two intersections at once [6].

2. Research Methods

In this work, a smart traffic light controller is developed to adjust the light sequences of traffic lights of two adjacent intersections based on the congestion level. The design of a smart traffic light controller can be divided into two phases which are the front-end design of the smart traffic light controller and the back-end design of the smart traffic light controller. Figure 1 shows the flowchart of the design methodology.

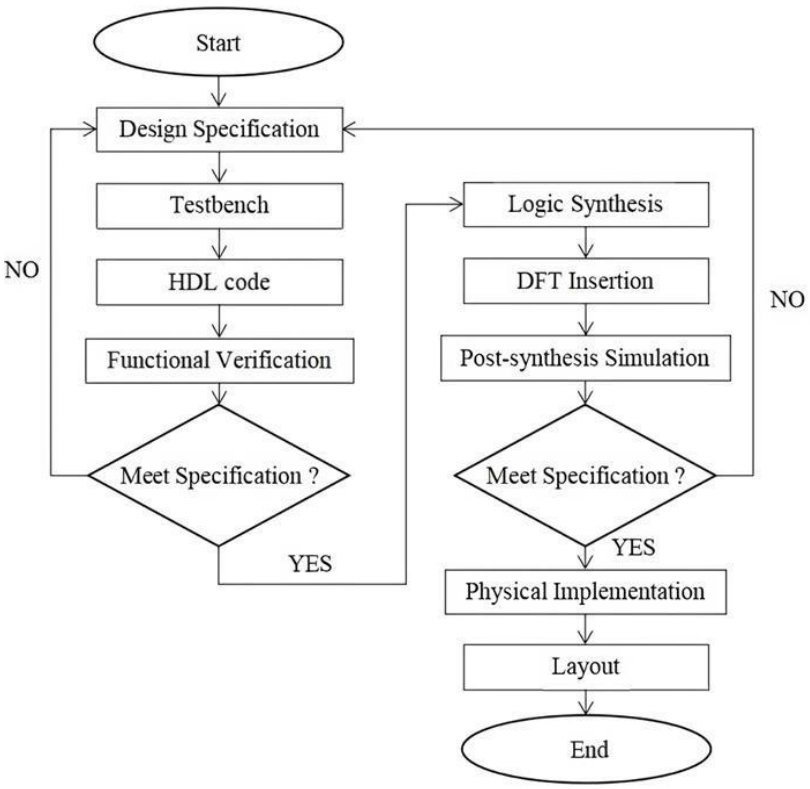

Figure 1: The flowchart of design methodology

2.1 Front-End Design of Smart Traffic Light Controller

The first phase of the work is the front-end design of the smart traffic light controller. In this phase, the design specifications of the smart traffic light controller must be justified to ensure the design of the smart traffic light controller operates according to the expectation. Verilog hardware description language (HDL) and testbench are written according to the design specifications of the smart traffic light controller. Functional verification is then carried out to verify that the design conforms to the design specifications. If the initial design does not meet the design specifications, the whole process will start over again from the design specification stage. If the design meets the design specifications, the work will proceed to the second phase which is the back-end design of the smart traffic light controller.

2.2 Road Structure

The road structure of the traffic intersection in this work is extracted from a traffic intersection that is in Ipoh, Perak illustrated in Figure 2. There are eight traffic movements represented by L1, L2, L3, L4, L5, L6, L7, and L8. L1, L2, L4, L5, and L6 are the main roads while L3 and L7 are the minor roads. Smart traffic light controller is based on the conditions and the traffic congestion level of each road to decide the time taken for each traffic light to stay green.

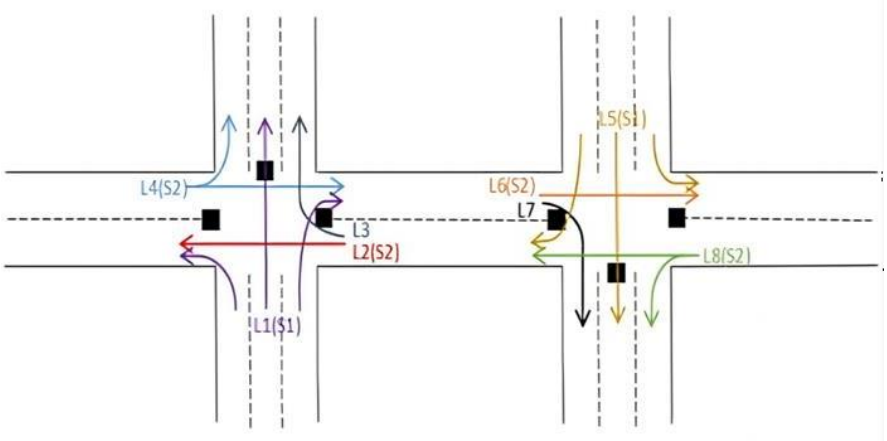

Figure 2: Road structure of traffic intersections

2.3 Time Taken for Traffic Lights to Stay Green

The time taken for traffic lights to stay green is decided by the congestion level of the respective road. The traffic lights of L1 and L5 will turn green at the same time because both roads are related. The time taken for the traffic lights of L1 and L5 is decided based on the congestion level of related traffic, S1. The congestion level of related traffic, S1 will be generated by taking the highest congestion level of L1 and L5. Table 1 shows the congestion level of related traffic, S1 (L1 and L5) and the time taken for traffic lights to stay green.

Table 1: Time Taken for Traffic Lights (L1 and L5) To Stay Green

Congestion Level of Related Traffic, S1 (Level)	Time taken for traffic light to stay green (s)	Binary Digit
1	0	00
2	20	01
3	40	10
4	60	11

While the traffic lights of L2, L4, L6, and L8 will turn green at the same time because the roads are related. The time taken for the traffic lights of L2, L4, L6, and L8 are decided based on the congestion level of related traffic, S2. The congestion level of related traffic, S2 will be generated by taking the highest congestion level of L2, L4, L6, and L8 to reduce the traffic congestion. Table 2 shows the congestion level of related traffic, S2 (L2, L4, L6, and L8) and the time taken for traffic light to stay green.

Table 2: Time Taken for Traffic Lights (L2, L4, L6 and L8) To Stay Green

Congestion Level of Related Traffic, S2 (Level)	Time taken for traffic light to stay green (s)	Binary Digit
1	0	00
2	20	01
3	40	10
4	60	11

2.4 Block Diagrams

Figure 3 illustrates the functional block diagram of the smart traffic light controller. There are five inputs in timer selector ‘timer_sel’ which are 60s, 40s, 20s, 15s, and 3s. The inputs are all in six bits. One of the inputs will be selected before the input is loaded into the counter. Once the timer is enabled, tEn=1, the countdown will begin. When the counter counts until ‘0’, t_out will be sent into the next state logics as the output. The outputs from deep Q-learning will be transmitted into next-state logics as inputs together with t_out (deep Q-learning is not part of this work. We assume that the outputs from the S1, S2 and S3 are provided by deep Q-learning). Finally, the output logics will generate outputs in L1, L2, L3, L4, L5, L6, L7, L8, ‘tEn’ and ‘t_sel’. Figure 4 shows the combination of the counter and the controller to form a complete smart traffic light controller. The outputs of the controller in L1, L2, L3, L4, L5, L6, L7, and L8 are represented in three bits which are ‘000 = red’, ‘010 = yellow’ and ‘100 = green’.

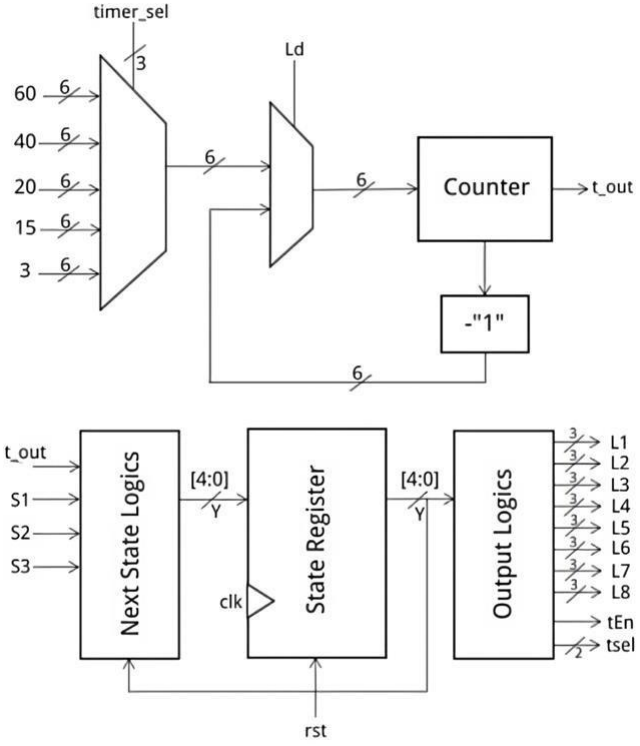

Figure 3: Functional block diagram of smart traffic light controller

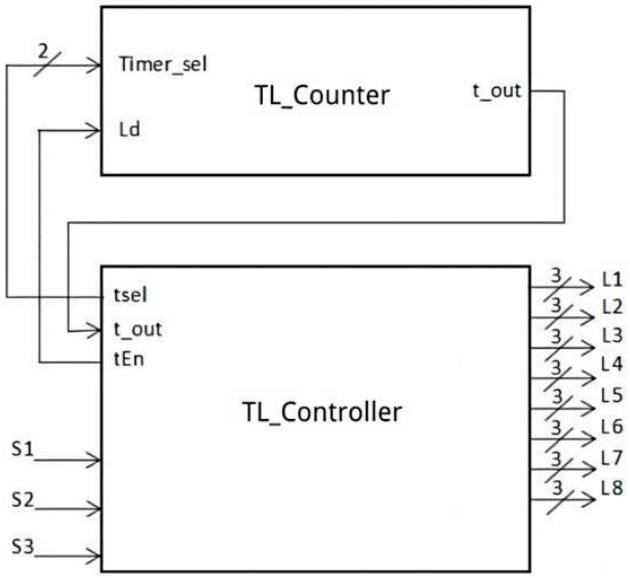

Figure 4: Block diagram of complete smart traffic light controller

2.5 Back-End Design of Smart Traffic Light Controller

The back-end design of the smart traffic light controller is operated by utilizing the 32nm technology and the saed32lvt_ss0p95v125c library. The back-end design of smart traffic light controllers begins with a logic synthesis that takes place to produce an optimized logic circuit from the front-end design. In the Design for Testability (DFT) insertion stage, scan insertion is carried out to enhance the testability of the controller. This involved integrating scan chains into the design to enable efficient testing of the circuit. A post-synthesis simulation is then conducted to verify that the circuit meets the design specifications after synthesis. The simulation is performed using the optimized logic circuit generated during logic synthesis. If the design does not meet the design specifications during the post-synthesis simulation, the entire process will start over again from the design specification stage. This iterative process would involve refining the design and re-performing logic synthesis. However, if the design meets the design specifications after the post-synthesis simulation, it proceeds to the physical implementation stage, which includes floor planning, placement, and routing where the layout is produced. By utilizing the 32nm technology with the saed32lvt_ss0p95v125c library throughout the back-end phase, we aimed to optimize the design for power, performance, and area, ensuring the efficient functioning of our smart traffic light controller [8].

2.6 Clock Gating Technique

In this work, logic synthesis operation optimizes the power consumption by utilizing a clock gating technique to selectively enable or disable clock signals based on activity. By inserting clock gating cells during synthesis, inactive portions of the circuit can have their clock signals turned off, reducing unnecessary switching and power consumption. Power estimation, technology mapping, and clock tree synthesis are employed to optimize power distribution. Validation ensures power targets are met. Clock gating effectively conserves power, improving power efficiency, extending battery life, and reducing thermal dissipation in electronic systems.

3. Results and Discussion

In this work, the results of testbench simulation, logic synthesis operation, and physical implementation of smart traffic light controllers are discussed. A smart traffic light controller has been developed to optimize the traffic flow management of two adjacent intersections based on traffic

congestion. The HDL code of the smart traffic light controller has been written according to the design specifications, block diagrams and algorithm state machine (ASM) chart. The functionality of the smart traffic light controller has been verified through the testbench simulation. The RTL design has been converted into a gate-level netlist through logic synthesis operation. Then, the gate-level netlist is converted into a physical layout that can be sent for IC fabrication through physical implementation operation.

3.1 Simulation Results

The testbench simulation of the smart traffic light controller is performed in ModelSim. A few conditions have been set to verify the functionality of the smart traffic light controller. There are five cases of testbenches in the testbench simulation. Table 3 shows the testbench simulation for each case.

Table 3: Cases of Testbench Simulations

Case	Input (S1)	Input (S2)	Input (S3)	Traffic Condition
1	01	00	0	The traffic lights of L1 and L5 will stay green for20s while others stay red.
2	00	10	0	The traffic lights of L2, L4, L6, and L8 will staygreen for 40s while others stay red.
3	11	01	0	The traffic lights of L1 and L5 will stay green for 60s while L2, L4, L6, and L8 will stay green for 20safter L1 and L5 turn red. L3 and L7 remain red.
4	10	00	1	The traffic lights of L1 and L5 will stay green for 40s while L3 and L7 will stay green for 15s after L1 and L5 turn red. L2, L4, L6, and L8 remain red.
5	01	01	1	The traffic lights of L1 and L5 will stay green for 20s then followed by L2, L4, L6, L8 for 20s. L2, L3, L6, and L7 will stay green for 15s after the restare red.

In order to prove that the functionality of the smart traffic light controller is the same as the cases in Table 3, some results of the testbench simulation are shown in Figures 5 to Figure 9. The results of the testbench simulations are shown in Figure 5 to Figure 9 respectively.

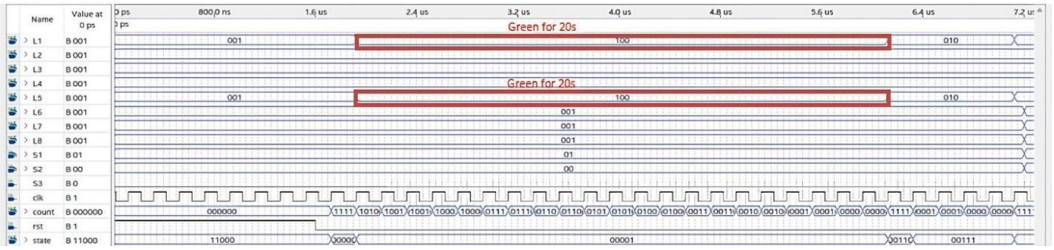

Figure 5: Testbench simulation for Case 1

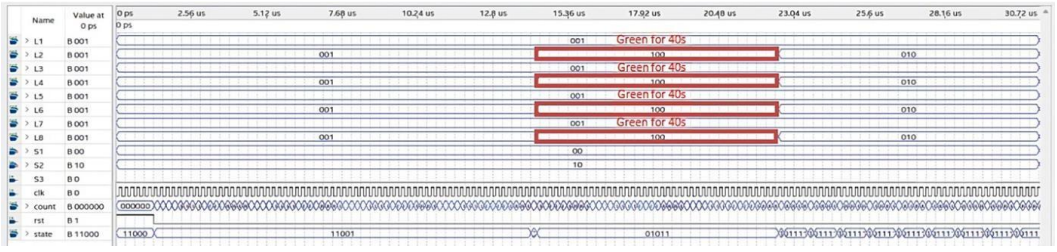

Figure 6: Testbench simulation for Case 2

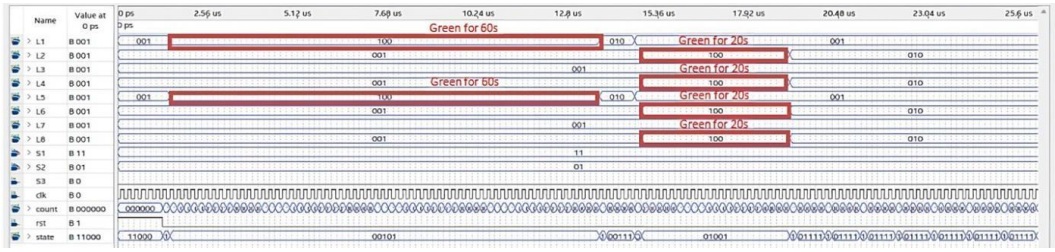

Figure 7: Testbench simulation for Case 3

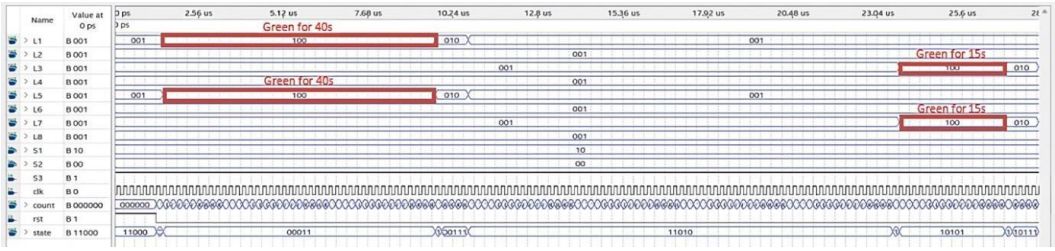

Figure 8: Testbench simulation for Case 4

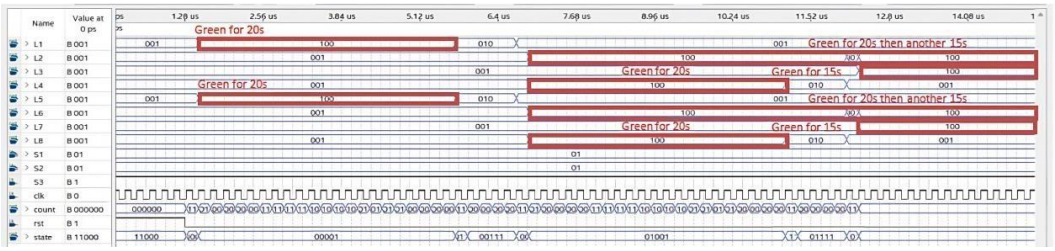

Figure 9: Testbench simulation for Case 5

3.2 Design Synthesis Results

Logic synthesis is performed by using Synopsys Design Compiler (DC) after the Verilog code has been verified. Logic synthesis is used to optimize and convert the Verilog code (RTL code) into a Gate-level netlist. In logic synthesis, the RTL design is analyzed and elaborated. At the same time, constraints are applied to the RTL design before the RTL design is sent for optimization and compilation. Once the constraints are set, logic synthesis operation is proceeded with optimization and compilation. At the end of the synthesis process, inspection is done to inspect the results of synthesis.

The final step of the synthesis process, the design is analyzed to ensure the design meets the design constraints. Reports are generated to analyze whether the design meets the design constraints. First, the area report is generated to obtain the area of the design. In this work, we obtained the total area of 496.4µm2. Next, the power reports are generated to obtain the total power, switching power, leakage power and internal power before the implementation of the clock gating technique and after the implementation of the clock gating technique. Table 4 illustrates the result of the power report which gives the total power consumption of the design before the implementation of the clock gating technique and after the implementation of the clock gating technique.

Table 4: Power report after design synthesis

Power	Before Clock Gating	After Clock Gating
Leakage power (pW)	1.2486e+08	1.1754e+08
Internal power (uW)	21.1173	20.8557
Switching power (uW)	0.7632	0.7148
Total power (uW)	146.7409	139.1144

By referring to Table 4, it is evident that the power consumption of the smart traffic light controller has been optimized through the implementation of the clock gating technique. Specifically, the leakage power has decreased by 5.8626%, internal power has decreased by 1.2388%, and switching power has decreased by 6.3417%. As a result, the total power consumption has been reduced by 5.1973%. These findings demonstrate the successful utilization of clock gating for power optimization in the smart traffic light controller. Finally, timing reports of the design are generated to ensure that the design meets the design constraints. Positive slacks from the generated reports indicate that the design meets the timing constraints.

3.3 Physical Implementation Results

Physical implementation operation on a netlist is performed by using Synopsys IC Compiler (ICC) after the netlist has been generated in logic synthesis operation. In this project, physical implementation is operated to take in a gate-level netlist and convert it into a physical layout that can be sent for IC fabrication.

The layout schematic of the design is generated through the physical implementation operation. There are several processes to generate the layout of the design which are partitioning, floorplanning, placement, clock tree synthesis, signal routing, and timing closure. In this work, the layout was successfully generated as shown in Figure 10.

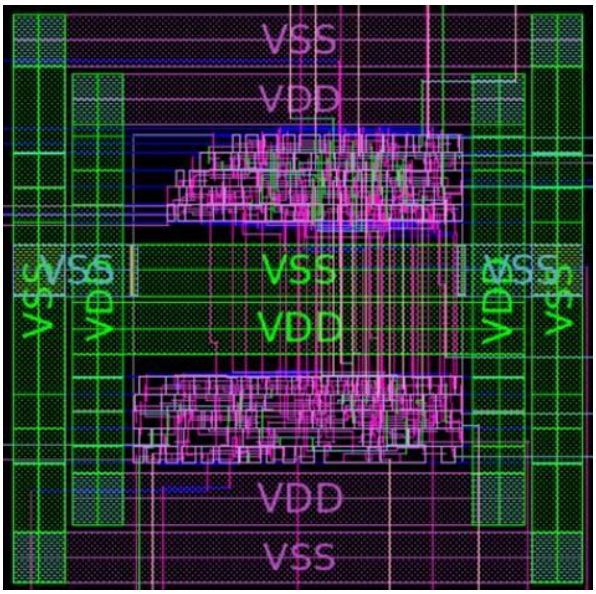

Figure 10: Layout of the design after placement and routing

3.4 Discussion

Based on the results, the smart traffic light controller has been successfully developed. It shows that the smart traffic light controller can manage the traffic of two neighboring intersections by adjusting signal timings based on congestion levels. The smart traffic light controller improves flow and efficiency of the traffic by coordinating the signals of both intersections, the controller optimizes the timing of green lights to minimize congestion and facilitate the smooth movement of vehicles. This coordinated approach ensures that traffic can flow seamlessly through both intersections, reducing delays and improving overall travel times [9].

On the other hand, the smart traffic light controller can respond to real-time traffic congestion and adjust signal timings accordingly. By continuously monitoring congestion levels, the controller allocates more green time to the intersection experiencing higher congestion. This dynamic adjustment

helps to maintain a balanced flow of vehicles through both intersections [9]. Additionally, the smart traffic light controller enhances safety by effectively managing traffic at adjacent intersections. The synchronized timing of traffic lights reduces the likelihood of conflicts and accidents. It ensures that vehicles can navigate the intersections smoothly, minimizing the risk of collisions or dangerous maneuvers [10].

Finally, the smart traffic light controller offers flexibility to adapt to changing traffic patterns. During peak hours or special events when traffic demands fluctuate, the controller can modify signal timings accordingly. This adaptability helps maintain efficient traffic flow and minimizes congestion during varying traffic conditions [10].

4. Conclusion

Overall, the smart traffic light controller that manages neighboring intersections provides numerous advantages for traffic management. It improves the overall management of traffic by optimizing the coordination between adjacent intersections, resulting in a smoother and more efficient transportation system. This enhances flow efficiency, reducing delays for drivers and minimizing traffic congestion. The controller also enhances safety by effectively managing traffic at the intersections, reducing the risk of accidents. Additionally, it offers adaptability to changing traffic patterns, allowing for timely adjustments to signal timings. In this work, we have provided the ASIC design of an adaptive smart traffic light controller. Furthermore, it has proved that the design is working based on the required specifications.

Acknowledgement

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