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VLSI Design for Low Power Home Automation and Security System Controller

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Abstract: The home automation system results from the rise of the automation era, which promotes the quality of living and energy resources savings. The current popularity of the home automation system is low as it hindered by its system complexity, complex user interface, power consumption, costing, absence of a security system and no backup power. Thus, this study aims to develop a compact home automation and security system controller consisting of environment comfort control, security system, and automatic load transfer switch system to archive a low power consumption. Very Large-Scale Integration (VLSI) design processes such as front-end and back-end were used for this project design via Synopsys EDA tools. At the same time, careful analysis of the performance and constraints were done to ensure no timing violations and physical design violations. The final layout's total power consumption was successfully lowered from the front-end design to 65.61µW. A positive timing slack of 1.95ns is obtained for the final layout of the design. Meanwhile, the final layout's dynamic power and leakage power is lowered by 4.67µW and 0.31µW, respectively, compared to the front-end process. The proposed design is successfully designed in low power and all the system functioned correctly concerning the input stimuli given under 100MHz.

Keywords: Home Automation System, Security System, VLSI, Low Power

1. Introduction

The advancement of technology results in the rise of the automation era whereby home automation system upgrades the standard and quality of living environment ranging from comfort, security to notable energy savings and other resources. Home automation system provided simultaneously control to home devices such as lights, electronic doors, fans, etc., using a central control unit whereby and hardware sensors act as the eye of the system to monitor and control the devices [1]. For example, the light of the house is controlled by the light intensity detected by the hardware sensor. The demand for home automation has risen steadily due to the necessity for a safe and comfortable living environment along with constant monitoring functionality, especially among the elderly and handicapped people. A total of 1.5 million home automation systems were installed in the United States in 2012 [2]. In [3],

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adopting the home automation system among the elderly people in Malaysia is growing where this demographic trend is expected to rise 6.5% in the coming years. The hindrance of this popularity might be due to the complexity of the system, power consumption, costing, complex user interface for elderly and handicapped people, not incorporated with a security system, and no backup power to prevent service interruption under power failure events.

Very Large-Scale Integration (VLSI) technology had been a trend design and created integrated circuit (IC). It enables the designer to develop a highly compact design with most functionality integrated into a complete system. Millions of transistors are packed into a single chip with a smaller die size [4]. The advancement of the VLSI technology leads the System-On-Chip (SoC) to be fabricated. The SoC application is a suitable platform for developing a compact home automation system such that multiple system and various I/O can be implemented into the same ship and, in turn, reduce the number of components of the system and the costing [5]. In previous research, Field Programmable Grid Array (FPGA) and Application Specific Integrated Circuit (ASIC) had been used for designing the mechanized home system.

Sharma et al. [6] proposed a simple home automation system using FPGA to control the operation of several home appliances such as sliding door, air conditioner and compound light only via sequence detection methodology. The security features are absent from this system. S.A.Sudiro et al. [7] used only two sensors, such as PIR and LDR, to develop a mechanized controller that regulates indoor lighting and the speed of the fans in a room only. Security system is not implemented in their proposed design. In contrast, the lighting control lacks some algorithm that enables automated switching day and night. N. Parvin et al. [8] develop home automation with comfort and security system via FPGA and generated the layout of the design using Mento Graphics. This proposed system enhances the security features in [9] in terms of user identifications and automatic door locking system while integrated the comfort system which absence in [9]. However, the proposed system only focused on temperature management of air conditioning, and the automatic door locking system caused the door to be locked up after a short period. In [10], an intelligent home model using ASIC technology had been developed by implementing six various sensors as input to control the two main features:1) Comfort 2) Security.

This project had the aim to develop a compact automated home controller with a low power consumption design that integrates the three main features: 1) Comfort, 2) Security, 3) Power Failure Prevention using VLSI technology. Total power consumption of the IC is notable contributed by the cell leakage power and dynamic power dissipation. This leads the leakage power and dynamic power to be considered the vital design parameter. As the size of the chip scaled down, its density and complexity will be increased result difficulty of designing high performance and low power consumption IC [11]. Thus, critical design parameter such as the leakage and dynamic power had been taken into account in this project.

2. Design Methodology

VLSI design process implemented in this project had been divided into two phases which is front-end design and back-end design. The Register Transfer Level (RTL) logic of the design had been simulated and set-up with a clock period of 10ns as the frequency constraint.

2.1 Front-end design

The front-end design started with the RTL logic development using Verilog code after determining the system's specification. The integration of the three main systems: 1) Environment comfort system, 2) Security system 3) Automatic load transfer switching system was developed using the hierarchical methodology. This hierarchy enabled the small units of blocks to be performed and compiled into the highest-level hierarchical block for providing a compact solution for realizing the complex system. Figure 1 shows the block diagram of the system of the proposed design where the dotted line indicating the top-level module of this project. After functional verification of each block using Synopsys VCS, the RTL logic design had been translated into the gate-level netlist and saved in the .ddc file via Synopsys Design Compiler. A specific unit library which is *cb13fs120_tsmc_max 90nm*, is used to perform logical synthesis using Design Compiler. Design constraints such as time, power and area were

used to optimize the gate-level netlist. The power had been optimized in high effort by increasing the number of iterations for the extra optimization. The flow of the front-end design is described in Figure 1.

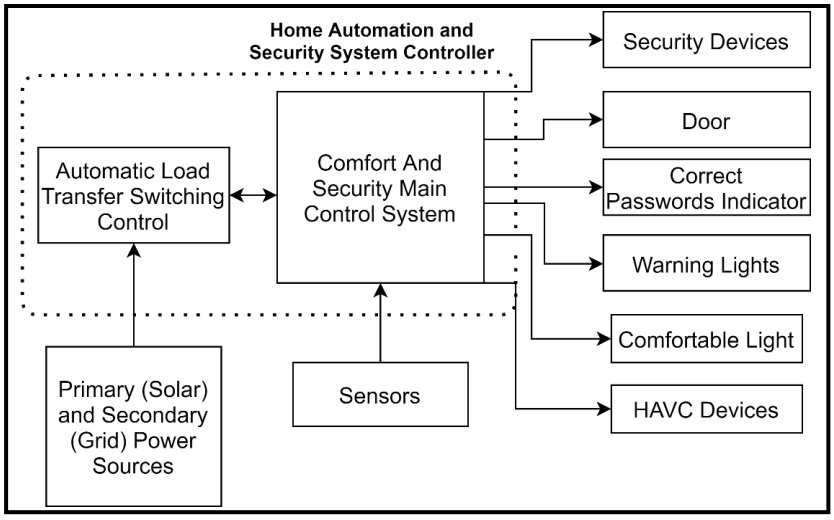

Figure 1: Block diagram for the home automation and security system controller

2.2 Back end design

Figure 2 described the back-end design started with the physical design using Synopsys IC Compiler with the *cb13fs120_tsmc_max 90nm* library. The milky way design library, which contained technology file information, reference libraries and initial design cell, is created at the very first place for the IC Compiler data setup. Next, the TLU+ Parasitic RC model files are specified and checked before load the .ddc file into the IC Compiler. After creating the floorplan, the standard cells are placed into the core area with leakage power optimization followed by Clock Tree Synthesis (CTS). Routing is then performed for routing the signal nets by involving the pre-route, global routing, track assignment and detailed routing. Power optimization is done again within this phase. Finally, the design layout is performed, and the design is verified via Design Rule Check (DRC) and Layout Versus Schematic (LVS).

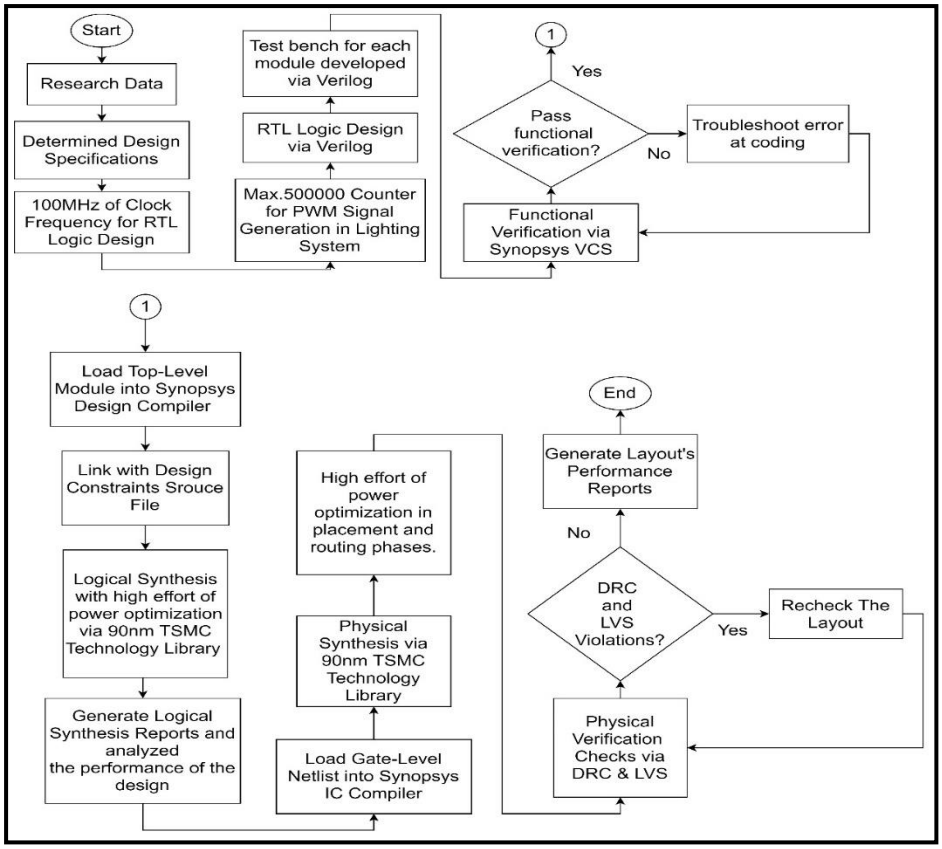

Figure 2: Flowchart for the home automation and security system controller design

3. Results and Discussion

3.1 Top-level module

Figure 3 shows the output waveforms for the top-level module in a clock period of 10ns after functional verification using Synopsys VCS. This module had successfully integrated the three main features. At the same time, it gives the corresponding output according to the input given by the sensors such as LDR, temperature sensor, magnetic switch, IR sensor, smoke sensor, input passcode and voltage inputs. For the environment comfort system, the light can be turned off in the day even with the presence of humans and able to adjust the light intensity in the night with 40% (no motion detected) and 100% (motion detected). The temperature management is implemented to control the actuators like heater, fan and air conditioner.

Moreover, user identification is implemented along with the fire alert system for the security system. The window alarm system is implemented in the system as well. The security devices such as the door alarm, window alarm, warning light (red light), and wrong password alert (yellow light) will be activated once the trails counter count to three. In other words, only two times of wrong user identification is allowed. The system managed to prevent service failure during power outages by mechanized switching between primary (Solar) and secondary (Grid) power sources. If the default Solar voltage is not in the range of 200V to 240V, the system will choose the grid powerline and vice versa. If each power is unstable, the system will connect the grid powerline to the load to allow the solar battery charged until the suitable voltage range.

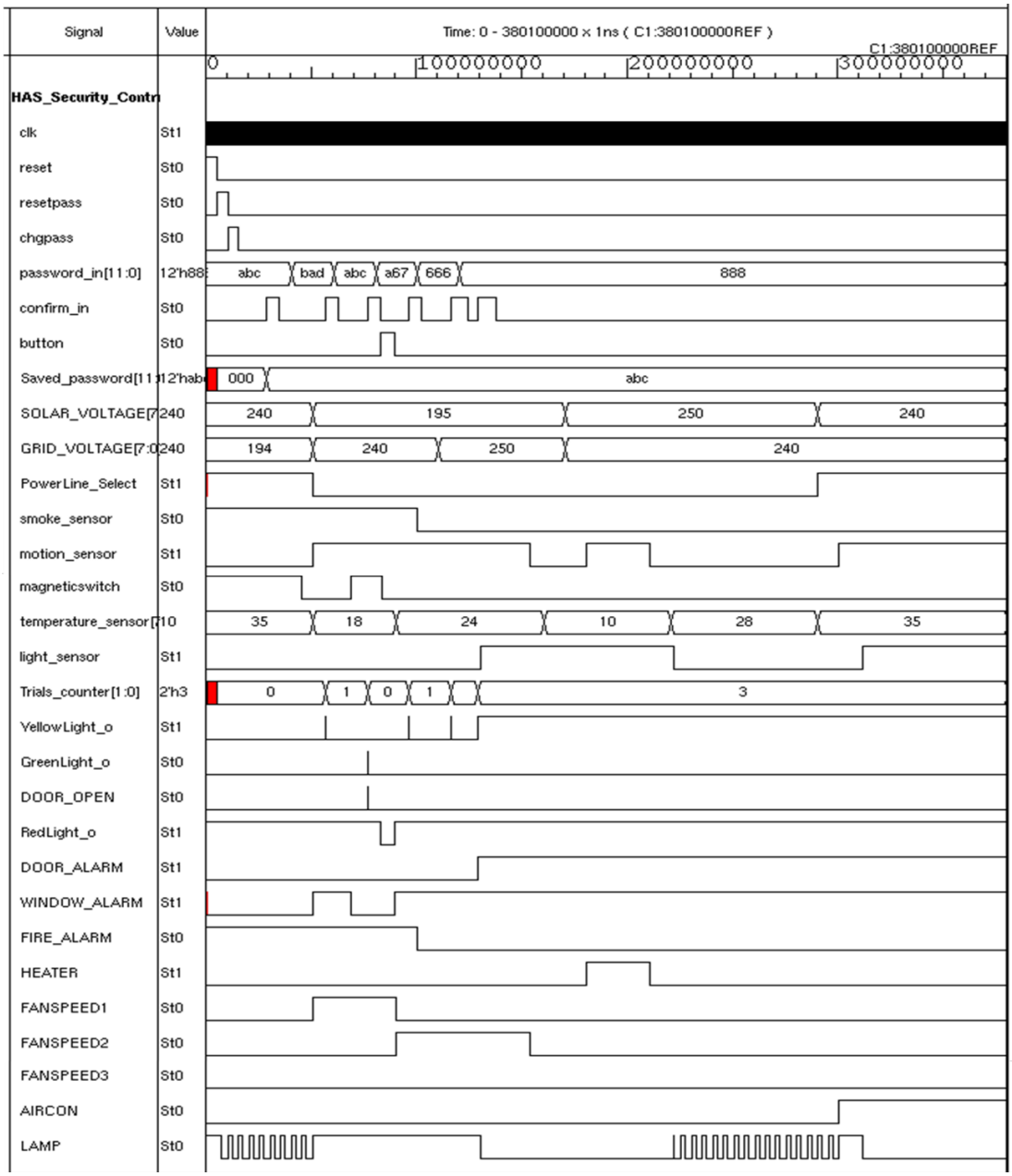

Figure 3: Output of the top-level module

3.2 Design compiler

Figure 4 shows the top-level module's RTL schematic view after performing logical synthesis using Synopsys Design Compiler linked with the design constraints. The design constraint, such as clock period of 10ns, expected clock network delay of 1ns skew, input and output constraints, operating

conditions, etc., were set for the design. Gate-level netlist is generated in this stage and exported as a .ddc file format.

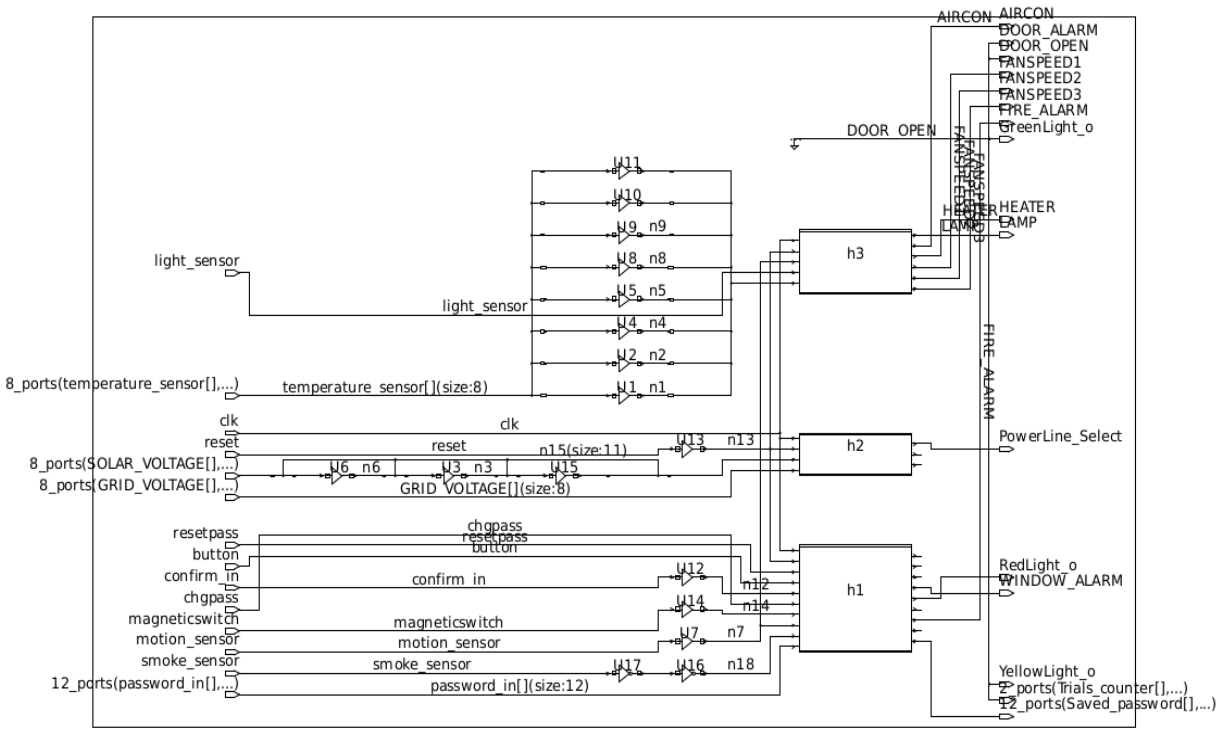

Figure 4: RTL schematic view of the top-level module after logical synthesis

Static timing analysis and statistical power analysis had been executed to analyze the performance of the design at the front-end design phases. The results obtained are shown in the Table 1. No timing violations such as setup and hold are reported at this stage, whereby a positive timing slack had been obtained. In other words, the data arrived time is lower than the data arrival time. The design had an area of 664.51 μm^2 with a total power consumption of 70.59 μW. The total power consumption of the design is contributed by a total of 67.22 μW dynamic power and a total of 3.37 μW cell leakage power.

Table 1: Performance report using Design Compiler

Metrics	Results
Timing Slack (ns)	1.88
Total Power (μW)	70.59

3.3 IC compiler

Table 2 shows the static timing analysis, statistical power analysis and area which obtained after the physical design using IC Compiler. The total power consumption of the design had been successfully reduced in the back-end design process as well as the area as compared to the results obtained in Table 1. The total dynamic power of the design in this back-end design phases is 62.55 μW which is 4.67 μW lower than the front-end design phases using DC Compiler. 3.06 μW of the cell leakage power is reported and it is 0.31 μW lower as compared to the front-end design.

Table 2: Performance report using IC Compiler

Metrics	Results
Timing Slack (ns)	1.95
Total Power (μW)	65.61

4. Conclusion

Home automation and security system controller using VLSI design methodology had been successfully designed and implemented. Low power of the design is achieved such that the dynamic and cell leakage power successfully optimized in the back-end design of VLSI. No violations are detected upon the logical synthesis and physical synthesis. The final layout of design is successfully implemented a total power consumption of 65.61 μW with a timing slack of 1.95 ns.

Acknowledgement

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