Smart Traffic Light Controller for UTHM Main Entrance

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Abstract: A traffic light controller (TLC) system is used to safely control vehicles' movement on the road to avoid collisions happened especially at intersections. Traffic lights control traffic movement by allocating adequate time between users from different intersections in the area. Usually, all traffic lights on the major roads are controlled by a fixed-time control system, while the minor roads are controlled independently by sensors. This project aims to create an efficient traffic light controller system to manage T-junction roads' movement at the UTHM main entrance and to ensure optimum traffic use. During peak hours, when people go out or come back home, traffic is at the maximum capacity, and without an efficient TLC system, it always happened to be jammed. The problem arises due to the unbalanced traffic flow from the exit road of UTHM, which has fewer vehicles most of the time, but it can also be the most congested road, especially during peak hours. The existed TLC system cannot configure the jam level in any way. To solve this problem, this designed controller system, used infrared sensors to detect the presence of vehicles and also to detect the traffic condition by placing sensors at the minor roads. The level of traffic density on the minor road is determined by placing three sensors at a different point, in this case, the exit way of UTHM campus. The first sensor indicates normal traffic, the second sensor indicates medium traffic, and the third sensor indicates heavy traffic. The timers are set according to the jam levels, which will indirectly help drivers save their time on the road. This controller system is able to detect level of traffic density as well as promotes efficient waiting time for drivers. The results of this controlled system are obtained from ModelSim. Various test bench has been made to verify the functionality and performance of the controller system through simulation. The controller system is described in Verilog HDL using Altera Quartus II.

Keywords: Smart Traffic Light, Controller System, IR Sensors

1. Introduction

A traffic light controller (TLC) system is used to safely control vehicles' movement on the road to avoid collisions, especially at intersections. Traffic lights control traffic movement by allocating adequate time between users from different intersections in the area. TLC can be implemented using a microcontroller such as PLC or PC, FPGA, ASIC design and more. FPGA is a semiconductor device with programmable logic blocks and flip-flops that connect through electrically programmable to become any digital circuit or system. FPGA is used in this project to develop TLC systems that require a real-time operation. It also has many advantages over the microcontroller. FPGA has better performance in terms of speed, multitasking, ease to develop and better adaptability towards any changes in the future [1]. The primary goal is to manage T-junction roads' movement at UTHM main entrance and ensure optimum traffic use. Usually, all traffic lights on the main roads are controlled by a fixed-time control system, while the smaller roads are controlled independently by sensors. The idea behind this project is that the sensor able to detect the level of traffic density on the small road by placing three sensors at a different point, at each small road. The first sensor indicates light traffic, the second sensor indicates medium traffic, and the third sensor indicates heavy traffic. Furthermore, the controller system can also provide adequate waiting time at the intersection based on the traffic condition, which will help drivers reduce fuel consumption and indirectly help reduce the pollution that vehicles on the road admit.

Many research works have been done on traffic light controller using different controlling methods. M.Sabri and Husin have used FPGA based TLC systems by controlling the intersections and allocating effective waiting time between various users during peak and off-peak hours [1]. R. Selvakumar and Dr.S. Nirmala have used fixed cycle approach during peak and off-peak hours. The system prioritises ambulances, fire engines and VIP vehicles by using the Emergency module fed by RF (Radio Frequency) Modules [2]. Shashikant V. Lahade and S.R. Hirekhan create a system that can identify emergency vehicles at a specific road and prioritise the traffic on that particular road where emergency happened. It also finds out defaulter who crosses the red signal by capturing images using a camera [3]. WM El-Medany and MR Hussain used the fixed-time system during peak hours. During non-peak hours, they used the fixed-time system to controlled the main road and sensor for the smaller road [4]. Nour T. Gadawe and Sahar L. Qaddoori proposed an idea to controlled the intersection between a busy and less busy road, with a sensor for the side street and walk request button. The system also contains switches to control the traffic light manually. The intersection uses four timing parameters with the ability to change these parameters manually [5]. In this project, a hardware implementation design (FPGA) is used. The designed controlled system is described in Verilog HDL.

1.1 Road Structure

The road structure of the traffic intersection is shown in Figure 1. There are five traffic movements represented by L1, L2, L3, L4 and L5 to be controlled. L2 and L3 are the main roads while L1, L4 and L5 are the minor road. Both of the main roads do not have any sensor. L1 and L4 have only 1 sensor at each of the road and both of the IR sensors are represented by s1(L1) and s2 (L4). L5 is the only road that has three sensors which represented by s3(level 1), s3 (level 2), s3(level 3) that connected along the road to detect the level of traffic density. The traffic flows are symbolized by the arrow in Figure 1.
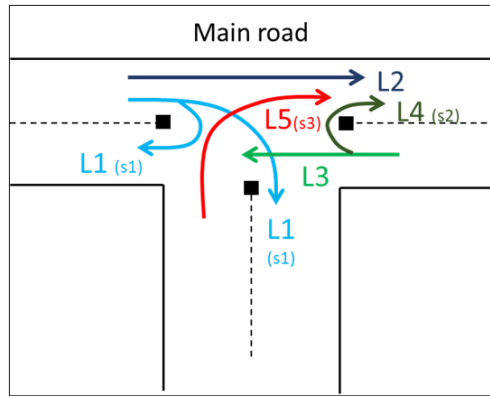
Figure 1: The T-junction Road at the UTHM Main Entrance

2. Methodology

Methodology focused on designing the smart traffic light controller. This is the most critical part of this controller design as it explained the block diagrams, ASM state machine.

2.1 Timer Setting

Timer is the most important factor that have to be set precisely and wisely in order to avoid potentially dangerous situations, such as a car accident at an intersection. Also, to make sure an efficient waiting time for drivers. This design is using fixed-time system but the timer settings are vary for depending on the traffic light conditions, whether the sensors are active or not.

2.2 Block Diagrams

Figure 2 shows the functional block diagram of the TLC system. The timer selector 'timer_sel' consists of five inputs with 6 bits which are 40s, 30s, 20s, 10s and 3s. It will select one of the inputs before loading it to the counter. The counter will start to countdown when the timer is enabled 'tEn=1' and results in 't_out' as the output. Then, 't_out' will enter the next state logics register along with the three sensors (s1, s2 and s3) before entering the state register. Finally, the output logic will show the output results in L1, L2, L3, L4, L5, 'tEn' and 't_sel'. Figure 3 shows the connections between the counter and the controller. The controller inputs are timer selector 't_sel', output of the counter 't_out', loader 'tEn and three sensors s1, s2 and s3. Sensor s1 and s2 have 1 bit, while sensor s3 has 2 bits. The outputs of the controller are traffic lights L1, L2, L3, L4 and L5. The traffic lights have 3 bits; '000 = red', '010 = yellow' and '100 = green'.
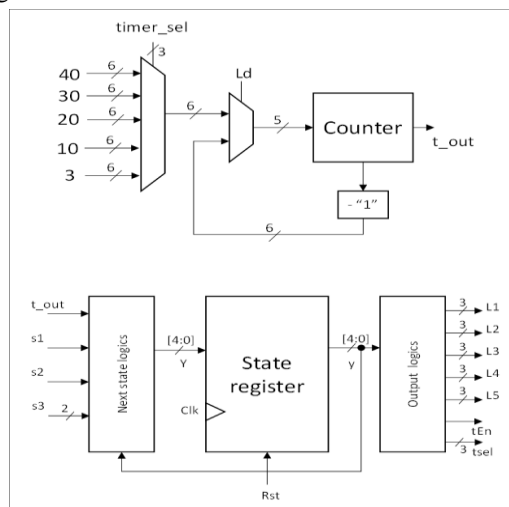

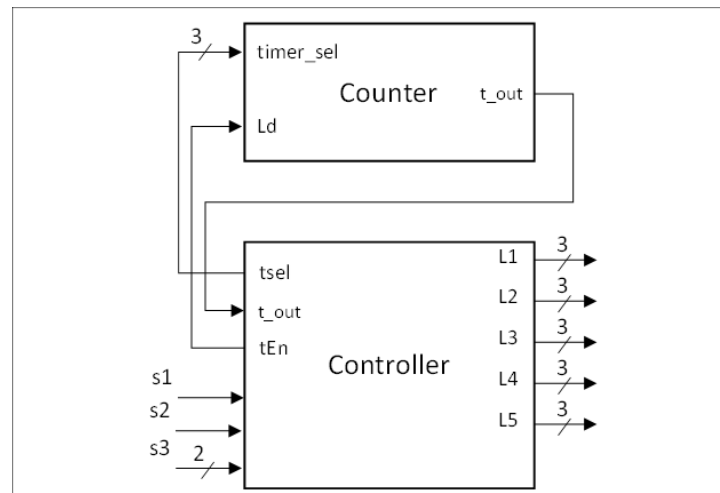**Figure 2: Functional Block Diagram (FBD) of the TLC System**

Figure 3: Functional block diagram of counter and controller

2.3 Algorithmic State Machine (ASM)

The state machine is the heart of the traffic light controller system. It controls the timer selector, timer loader, timer counter, sensors, and traffic lights sequence. The traffic light controller has 31 states.

Table 1 shows sensor two 's3' has 2-bits binary. When 's2 = 00', it means no vehicles in the queue, 's2 = 01' means the road is congested at level 1, 's2 = 10' means the road is congested at level 2, 's2 = 11' means the road is congested at level 3.

Table 2 shows the timer selector has 3 bits binary, but in the chart, 'tsel' is represented by a decimal number. When 'tsel = 0', the timer set to 40s, 'tsel = 1', the timer set to 30s, 'tsel = 2', the timer set to 20s, 'tsel = 3', the timer set to 10s, 'tsel = 4', the timer set to 3s. Sensor one 's1' has a 1-bit binary. 's1=1' means the sensor is activated while 's1=0' means vice versa.

Table 1: Function of S3

S3	Function
00	Not detect any vehicles
01	(normal traffic) level 1
10	(medium traffic) level 2
11	(Congested) level 3

Table 2: Input timer of 'tsel'

tsel	Time
0	40s
1	30s
2	20s
3	10s
4	3s

Table 3 shows the traffic lights conditions, which is red, green and yellow. The traffic light is in 3 bits binary. When the traffic light is '000', it means red. '100' means green, and '010' means yellow. Every change to a green state has 1s of a delay from the previous state for safety reasons. It is to avoid accident happens between interchange of lights for each traffic light.

Table 3: The traffic light condition

3-bits binary	Traffic light condition
001	Red
100	Green
010	Yellow

The sequence starts from reset, which is that all traffic lights will turn red. Then it continues with state zero (S0) until state three (S3). At S3, sensor 's1' will be check after the counter finish countdown S3. When sensor s1 detect vehicles (s1=1), traffic light L1 and L2 will continue to state S4 which is, both of the traffic lights will turn green for 20s. Considering traffic light L1 is the minor road, it will only green for 20s before turns yellow, while L1, the major road, will continue green for another 20s alone before turns to yellow. However, if sensor 's1' not detect any vehicles (s1=0), the controller will skip traffic light L1, and only traffic light L2 will green for 40s.

The controller continues the sequence until state thirteen (S13) and checks sensor two (s2). When s2 detects a vehicle (s2=1), the traffic light L3 and L4 will turn green for 20s. Traffic light L4 is the minor road, so it will only green for 20s before turns yellow, while L1, the major road, will continue green for another 20s alone before turns to yellow. If sensor s2 does not detect any vehicles (s1=0), only traffic light L2 will green for 40s.

Then the controller will continue the sequence until state twenty-three (S23). After the counter finished countdown S23, sensor three 's3' will be checked. 's3' connects three sensors altogether. This sensor is located specially at L5 (refer to Figure 1. 1). These sensors are placed at three different points to determine the condition of traffic at that moment. Referring to Table 3. 1, these sensors will detect three levels of traffic conditions on road L5, whether it has no vehicle at all, regular traffic (level 1), medium traffic (level 2) or heavily congested (level 3). So if sensor three is deactivated 's3=00', the controller will skip the sequence and back to state 0. When vehicles queue up to level 1 (s3=01), L5 will green for 10s. When vehicles queue up to level 2, and both sensors are active (s3=10), L5 will green for 20s, and when vehicles queue up to level 3 and all of the sensors are active, 's3=11', so L5 will green for 30s. After L5 turns yellow, the state will go back to S0.

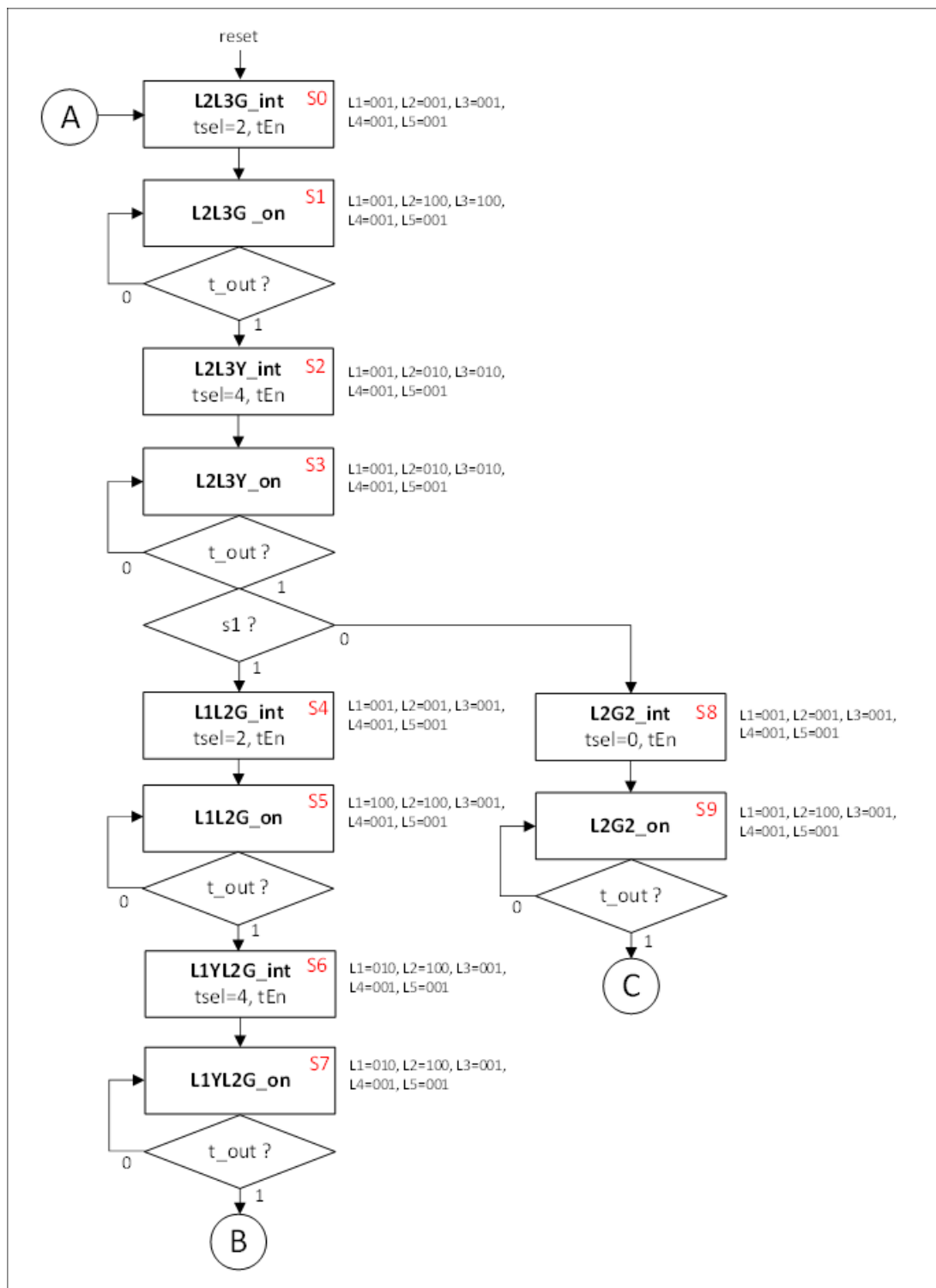Figure 4, Figure 5 and Figure 6 show the TLC system's continuous ASM charts.

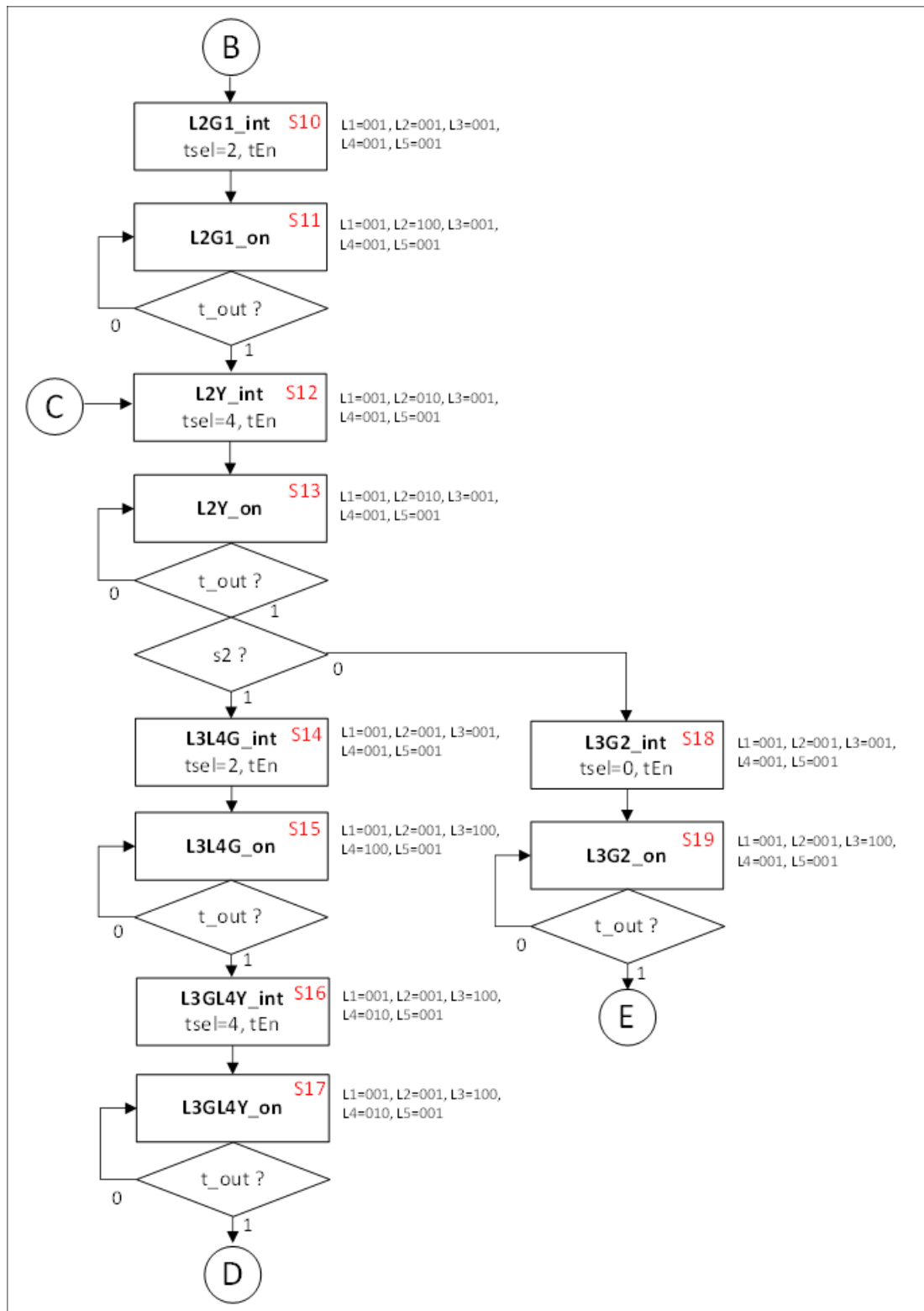**Figure 4: The ASM chart of the TLC system (part 1)**

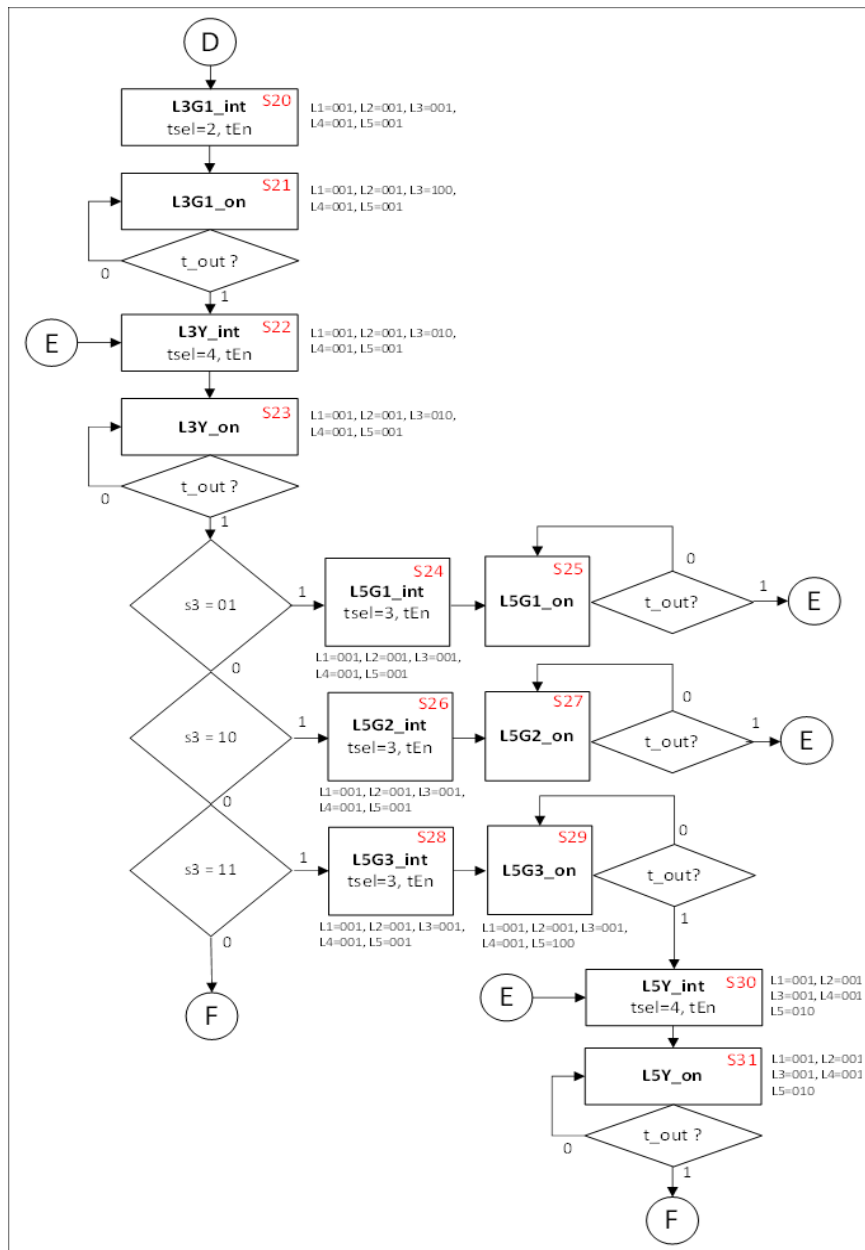**Figure 5: The ASM chart of the TLC system (part 2)**

Figure 6: The ASM chart of the TLC system (part 3)

3. Simulation Results

The test bench of the TLC system result is obtained using the combination of two software: Altera Quartus II and ModelSim Altera. This design consist few test bench to test varies traffic conditions.

3.1 Test Benches

This project consists of eight cases of test benches. Table 4 shows the list of test benches and traffic conditions. For Case 1, no sensor is triggered at roads L1, L4 and L5. Case 2, only sensor s1 on road L1 is triggered. Case 3, only sensor s2 on road L4 is triggered. Case 4, for sensors s1 and s2 on road L1 and L4, are triggered. Case 5, only sensor s3 level 1 on road L5 is triggered. Case 6, only sensor s3 level 2 on road L5 is triggered. Case 7, only sensor s3 level 3 on road L5 is triggered. Case 8, all sensors s1, s2 and s3 on roads L1, L4 and L5 are triggered. Case 8, sensors s1, s2 and s3 level 1 on road L1, L4 and L5 are triggered.

Table 4: List of test benches and traffic conditions

Case	Sensors		TL	Traffic condition
1	s1	0	L1	L2 green for 40s, L3 green for 40s
	s2	0	L4	
	s3	00	L5	
2	s1	1	L1	L1 and L2 green for 20s (S5)
	s2	0	L4	
	s3	00	L5	
3	s1	0	L1	L3 and L4 green for 20s (S14)
	s2	1	L4	
	s3	00	L5	
4	s1	1	L1	L1 and L2 green for 20s (S5), L3 and L4 green for 20s
	s2	1	L4	(S14)
	s3	00	L5	
5	s1	0	L1	Vehicles queue up to level 1 (normal traffic), L5 green for
	s2	0	L4	10s (S25)
	s3	01	L5	
6	s1	0	L1	Vehicles queue up to level 2 (medium traffic), L5 green for
	s2	0	L4	20s (S27)
	s3	10	L5	
7	s1	0	L1	Vehicles queue up to level 3 (heavy traffic = congested), L5
	s2	0	L4	green for 30s (S29)
	s3	11	L5	
8	s1	1	L1	L1 and L2 green for 20s (S5), L3 and L4 green for 20s
	s2	1	L4	(S14) and L5 green for 10s (S25)
	s3	01	L5	

3.2 Verilog HDL Synthesis Results

These are the results based on the test bench in Table 4. When the IR sensors are not detect any vehicles on the minor road, the controller will skip sequence automatically. The synthesis has successfully executed using ModelSim Altera. The simulation of each case is shown in Figure 7-14.
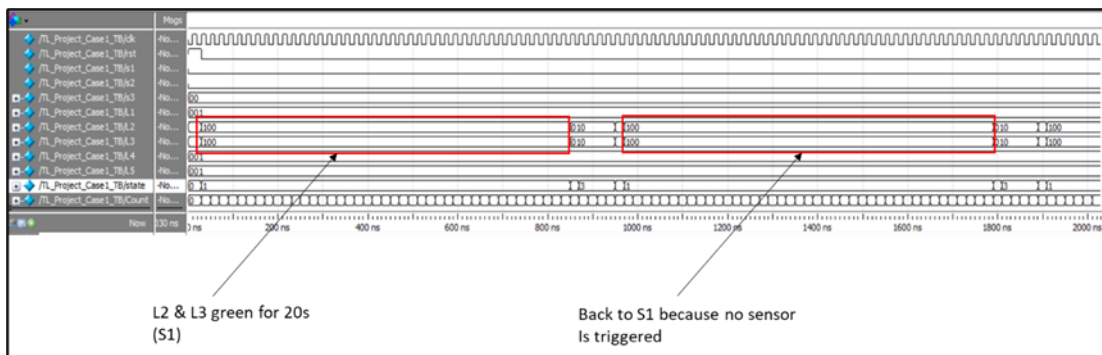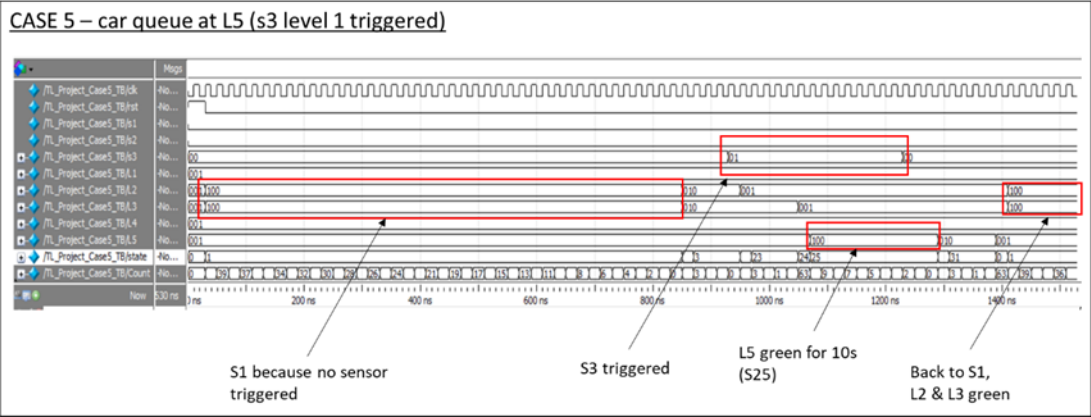

Figure 7: The simulation of Case 1
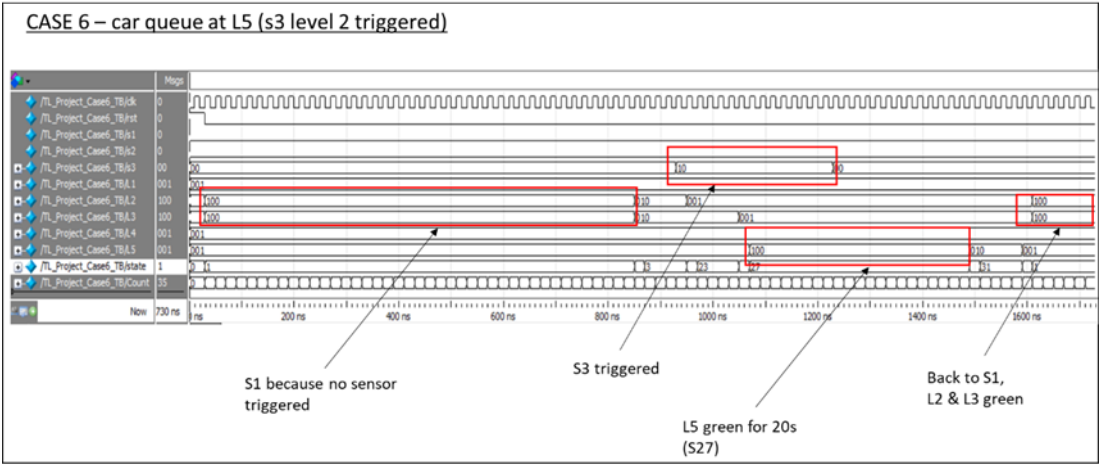
Figure 8: The simulation of Case 2

Figure 9: The simulation of Case 3

Figure 10: The simulation of Case 4

Figure 11: The simulation of Case 5

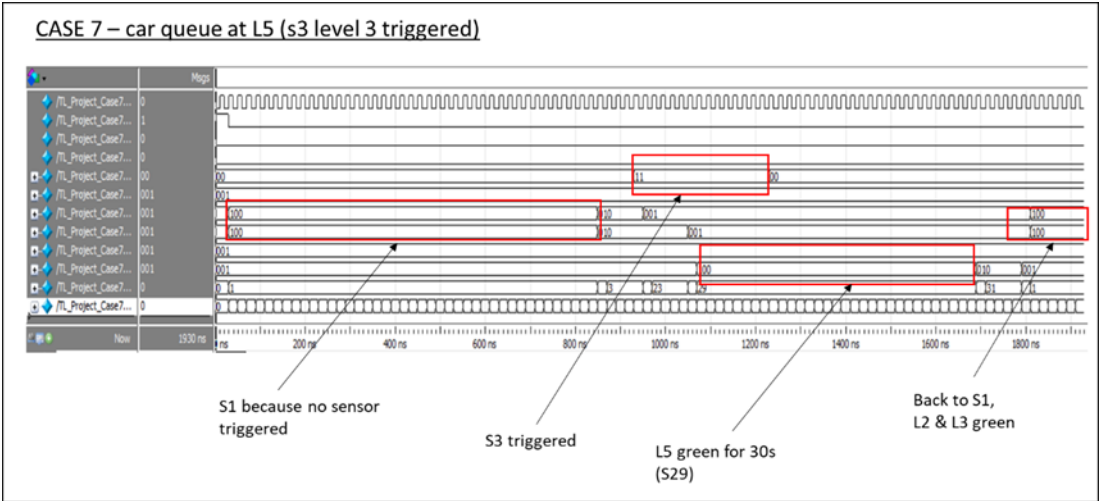**Figure 12: The simulation of Case 6**
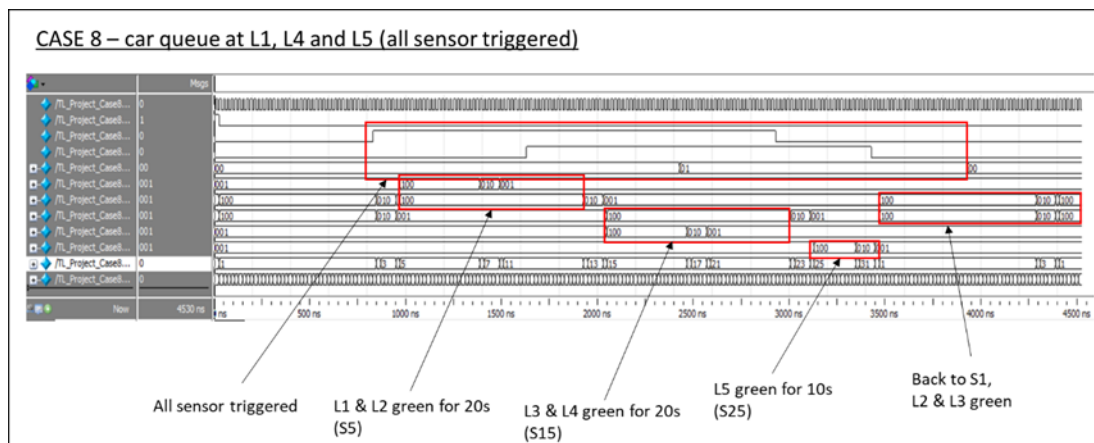

Figure 13: The simulation of Case 7

Figure 14: The simulation of Case 8

4. Conclusion

This TLC system is still using the fixed time systems but with few add-ons of sensors to detect the presence of vehicles and detect the level of traffic density that happen at the small road. To detect the level of traffic density, three sensors are placed on different points at road L5 to indicates the traffic condition at that moment. The first level indicates regular traffic, the second level indicate medium traffic, and the third level indicates heavy traffic. This project's idea was implemented based on the actual situation that usually happens during pick hours, especially at the exit road of UTHM.

A systematic traffic light controller is successfully designed for the T-junction at UTHM main entrance. All sorts of test bench are tested to verify the functionality and performance of the controller system. The designed controlled systems are verified through simulations in ModelSim Altera.

Acknowledgement

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