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Design of Reversible Binary Half and Full Adder/Subtractor Using Reversible Gates

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Abstract : The power consumption in classical computers has grown to be a critical issue. Thus, quantum computers have become a promising alternative to classical computers for more processing power and lower energy consumption. Reversible gates are important for building the quantum computers. Reversible circuits have various applications, such as digital signal processing, optical computing, quantum computing, etc. The design and synthesis of reversible gates and circuits have grown in popularity and attracted the attention of many researchers. The adder and subtractor are important computation blocks for the structure of the Arithmetic Logic Unit (ALU). In this paper, a design of reversible binary half and full adders and subtractors using reversible logic gates is proposed. The TR (Thapliyal Ranganathan) and Peres gates are used to construct the reversible half adder and subtractor circuit. Meanwhile, the Double Peres Gate (DPG), Fredkin, and NOT gates are used to build the reversible 1-bit full adder and subtractor circuit. The designs are optimized in terms of number of gates, constant inputs, garbage outputs, and quantum cost. The truth table representation and the Binary Decision Diagram (BDD) synthesis method are used to represent and synthesize the circuits, respectively. The circuits are synthesized and simulated using the Verilog Hardware Description Language code and Xilinx ISE 14.7. The results show that the proposed designs achieve the lowest quantum cost in both half adder/subtractor and full adder/subtractor. As the half adder/subtractor has six quantum cost and the full adder/subtractor has nine quantum cost.

Keywords: Full adder, Half subtractor, Garbage output, Quantum cost, Reversible gates

1. Introduction

Power dissipation is one of the most critical aspects of an irreversible circuit. According to Landauer's principle, the irreversible circuit produces heat dissipation of around *kTln2* Joules for every bit of missing information during the computation, where *k* is the Boltzmann's constant, and *T* is the absolute temperature [1]. In 1965, Moore proposed Moore's law which stated the total number of

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transistors doubles every 18 months in integrated chips. This led to an increase in the number of transistors. Hence, the processing power of computers has progressively increased due to the increasing density of transistors that leads to a growth in heat because of information loss during computing the data [2]. In 1973, C.H. Bennet proved that there would be no power loss in digital circuits when redesigning circuits using reversible gates [3]. As a result, researchers are looking for alternatives to classical computing, which is a quantum computing, as the demand for more processing power and lower energy consumption. Thus, this has become a major factor in developing reversible computing [4]. In reversible gates, there is no loss of power during reversible computation. Many technologies apply reversible logic, such as biotechnology, nanotechnology, adiabatic CMOS design, quantum computing, optical computing, etc. [5] .

Reversible gates generate a unique one-to-one mapping between inputs and output vectors and vice versa. In the reversible gate, the number of outputs are the same as the number of inputs [4,6,7]. Thus, fan-out and feedback are not allowed [8]. If necessary, some additional wires can be added to the inputs and outputs of a gate to make it reversible. The additional wires that are added to the inputs are called the ancilla (constant inputs) and the additional wires to the outputs are called garbage outputs.

In the reversible computers, the computational blocks are important circuits such as multiplexer, decoder, arithmetic logic unit, etc. [9]. The arithmetic units such as adders, subtractors, comparators, etc. have an effect on the performance and efficiency of the circuit. Thus, research is necessary to develop new design and synthesis approaches for the implementation of reversible arithmetic circuits [10,11].

Some researchers designed half and full adders/subtractors using existing reversible gates, while others made new gates then used them to construct the reversible half and full adder/ subtractor. Rohini et al. [12] designed a half adder and subtractor as two circuits. The Peres gate is used as the half adder and the CNOT, NOT, and Peres gate as the half subtractor. Both designs require a large number of quantum cost, which reduces the performance of the circuits. In 2018, Nayana et al. [13] proposed a half adder and subtractor circuit using two different gates. Meanwhile, Balaji et al. [14] used two Feynman Double Gates (FDG) and two Fredkin Gates. A new reversible gate, called R gate, was introduced by Montaser et al. [9]. They designed a reversible half adder/subtractor by using three R gates and manage to achieve 4 quantum cost. In actuality, the three R gates combine 3 NOT gates, 1 Toffoli gate, and 2CNOT gates. Thus, the quantum cost of the circuit will be 8. Furthermore, FGE* and SS are new gates introduced by Orts et al. [15] and Kolay et al. [16], respectively.

Many research have been done on designing the reversible full adder/subtractor circuits using existing reversible gates. In 2016, Shukla et al. [17] presented two designs for a reversible 8-bit adder-subtractor circuit. In the first design, the PFAG (Parity Full Adder Gate) gate is applied to construct the full adder circuit. Thus, the 8-bit adder/subtractor circuit is designed by cascading eight PFAG gates and eight Feynman gates. This design generated 17 garbage outputs and 72 quantum costs. In the second design, the 8-bit adder/subtractor circuit is designed by cascading eight WG gates. Then, [18] applied a different idea to construct a full adder/subtractor. It is built using the 3×8 reversible decoder and the Feynman gate. Further, the designs of reversible 32-bit BCD (Binary Coded Decimal) adders/subtractors have been attempted by Anjana et al. [19] depended on the parallel pipelined unit to improve the speed and the power. Some researchers have made comparisons over existing full adder and subtractor. In [20], many comparisons are made to realize the most efficient full adder circuits in terms of power, area, and delay. In 2020, interesting reversible ternary full adder and full subtractor circuits are proposed by Asadi et al. [10].

Many researchers have proposed different designs for reversible half and full adders/subtractors. However, the designs still need to be improved in terms of the number of garbage outputs, quantum cost, and constant inputs in order to obtain better performance and less complexity.

In this paper, a new reversible half adder/subtractor, also a new reversible 1-bit full adder/subtractor are presented using reversible gates. The most feature of the proposed designs is the optimization of the main criterions which are garbage outputs, gate counts, quantum cost, and constant inputs. The paper is organized of the following sections: the second section presents the basic reversible gates. While the proposed circuits are provided in the third section. The results and performance comparisons are presented in the fourth section. Finally, Section 5 provides a conclusion and future works.

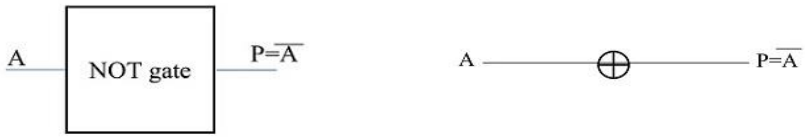
2. Basic Reversible Gate

A reversible gate is a digital circuit. It is a bijective gate. It has number of inputs equal to the number of outputs. Thus, it has a mapping one to one. The most terms that should be considered when designing and synthesis of reversible circuits are garbage output, quantum cost, constant inputs, and gate count [21]. The garbage output is the number of outputs that are not used as a primary output. They are necessary to achieve reversibility. While quantum cost refers to the cost of the number of primitive reversible gates. It is required to realize the circuit and it is important for implementation [22]. In addition, quantum cost is the total number of 1×1 or 2×2 reversible gates required to design the reversible gate or circuit. Thus, the quantum cost of a circuit is the total quantum cost of all gates which are built the circuit. Whereas constant inputs, also known as ancilla inputs, refer to the number of inputs that are assigned to be constant at either 0 or 1 to synthesize reversible gates and reversible circuits [12,23]. Meanwhile, the gate count refers to the total number of reversible gates used in a circuit. There are many reversible gates, such as the NOT gate, which is a 1×1 gate, and many 3×3 reversible gates, such as the Fredkin gate, Toffoli gate, Peres gate, and TR (Thapliyal Ranganathan) gate.

2.1 Not Gate

A NOT gate is the simplest reversible gate. It is a 1×1 gate with a quantum cost of zero. It has one input which is *A* and one output *P*, where the output is an inversion of the input. **Figure 1(a)** shows the symbol of the reversible NOT gate, which consists of input and output. **Figure 1(b)** shows the quantum representation which has a target symbol $(\oplus)$ works as an Exclusive OR operation. The target symbol in the NOT gate works as an inverter because the NOT gate has only one input. The equation of the NOT gate is given by

$$P = \bar{A} \quad \textbf{Eq. 1}$$



(a) (b)

Figure 1: Reversible NOT gate (a) symbol and (b) the quantum representation

2.2 Feynman Gate

A 2×2 Feynman gate [24] is also called a controlled-NOT gate (CNOT). It has the quantum cost of one. The Feynman gate can be used to copy the signal to avoid the fan out [11]. **Figure 2 (a)** shows the Feyman gate symbol. While **Figure 2 (b)** shows the quantum representation of the Feyman gate, which has the target symbol $(\oplus)$ and has a $(\bullet)$ that represents a control point. The control point passes the value from the input control to the associated output without any change. **Table 1** shows the truth table of the Feynman gate. The equations of the Feynman gate are given by

$$P = A \quad \textbf{Eq. 2}$$

$$Q = A \oplus B \quad \textbf{Eq. 3}$$

(a) (b)

Figure 2: Feynman gate (a) symbol and (b) the quantum representation

Table 1: Truth table of the Feynman gate

A	B	P=A	Q=A⊕B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2.3 Fredkin Gate

A Fredkin gate is a 3×3 gate [25] with mapped inputs (*A, B, C*) to outputs (*P, Q, R*). The quantum cost of the Fredkin gate is 5 [26]. The equations of the Fredkin gate are given by

$$P = A \quad \textbf{Eq. 4}$$

$$Q = \bar{A}.B + A.C \quad \textbf{Eq. 5}$$

$$R = A.B + \bar{A}.C \quad \textbf{Eq. 6}$$

2.4 Peres Gate

It is a 3×3 gate [27] with mapping (*A, B, C*) to (*P, Q, R*). The quantum cost of the Peres gate is 4 [28]. The equations in Peres gate are given by

$$P = A \quad \textbf{Eq. 7}$$

$$Q = A \oplus B \quad \textbf{Eq. 8}$$

$$P = (A.B) \oplus C \quad \textbf{Eq. 9}$$

2.5 Toffoli Gate

It is a 3×3 gate (TG), which is also known as a controlled-controlled not [29]. It has a quantum cost of 5. The equations of the Toffoli gate are given by

$$P = A \quad \textbf{Eq. 10}$$

$$Q = B \quad \textbf{Eq. 11}$$

$$R = (A.B) \oplus C \quad \textbf{Eq. 12}$$

2.6 TR Gate

A TR gate is a 3×3. The equations of the TR gate are given by

$$P = A \quad \textbf{Eq. 13}$$

$$Q = A \oplus B \quad \textbf{Eq. 14}$$

$$P = (A.\bar{B}) \oplus C \quad \textbf{Eq. 15}$$

2.7 Double Peres Gate

A 4×4 Double Peres Gate (DPG) has mapping inputs *A*, *B*, *C*, *D* to outputs *P*, *Q*, *R*, *S*. If the input *C*=0 and the input *D*= *Cin*, the DPG gate can be used as a full adder. The quantum cost of DPG is 6. The DPG gate is primarily used to reduce the garbage output. The DPG gate equations are given by

$$P = A \quad \textbf{Eq. 16}$$

$$Q = A \oplus B \quad \textbf{Eq. 17}$$

$$R = A \oplus C \oplus D \quad \textbf{Eq. 8}$$

$$S = (A \oplus B).D \oplus (A.B) \oplus C \quad \textbf{Eq. 19}$$

3. Methodology

3.1 Methods

The reversible logic implementation on half and full adder and subtractor circuits have been reported in several works and in various styles. In this work, some basic reversible gates are used to design reversible binary half and full adder and subtractor circuits.

The states of the circuits inputs are binary. Also, the constant inputs are added to the circuits, thus the best method to synthesis the circuits is the Binary Decision Diagram (BDD) which can reduce the complexity. The reversible gates are connected in a cascade manner. The truth table is used to represent and define the function between inputs and outputs of the circuits. The proposed designs are developed using the Verilog Hardware Description Language (VHDL) and are simulated and verified in Xilinx ISE 14.7. The waveforms are generated to verify the performance of both proposed designs. The following flow chart explains the circuits designs:

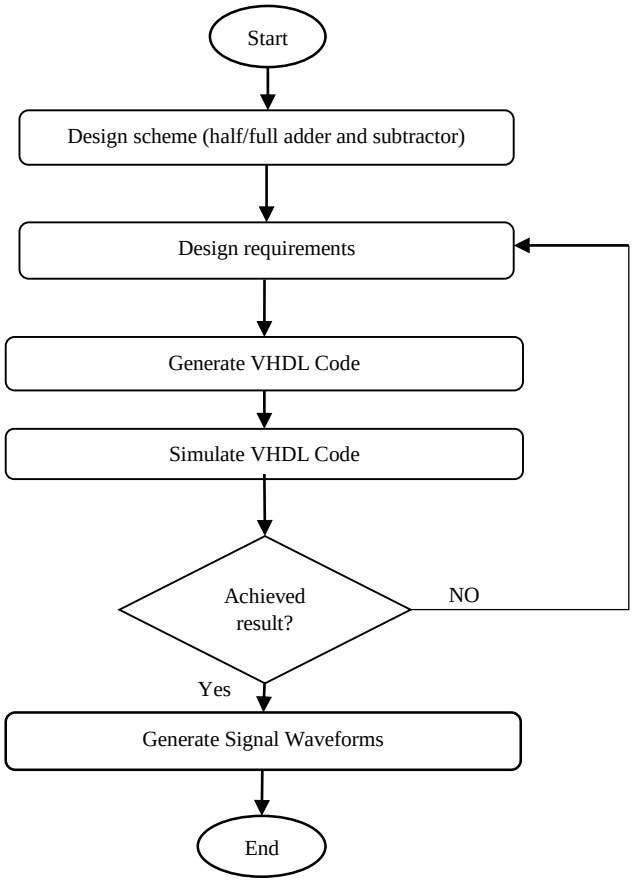


Figure 3: Flow chart of reversible binary half and full adder and subtractor

3.2 The Proposed Designs

In this sub-section, the reversible half and full adder/subtractor design of this work is discussed. The circuits are implemented using several reversible gates.

3.2.1 Reversible Binary Half Adder/Subtractor

The half adder/subtractor circuit is used to perform the addition and subtraction of two numbers. The reversible binary half adder/subtractor circuit is built using the reversible Peres gate and TR gate. The Peres gate is used to design the reversible half adder. It has less hardware complexity and less quantum cost [4]. Likewise, the TR gate is used to design the reversible half subtractor.

The half adder/subtractor circuit takes two binary numbers as the inputs, adds and subtracts them. Then it produces sum, sub, carry, and borrow as the outputs. Actually, the reversible adder/subtractor gates consist of three inputs and three outputs. Thus, the reversible binary half adder/subtractor circuit takes 3 bits inputs. The first two inputs (*A, B*) are the two bits required to be added or subtracted. The third bit (*C*) is a constant bit with a value of zero. The circuit returns five outputs. The first output is the summation bit, denoted by *SUM*. It is also the difference bit, calculated by **Eq.20**. The second output is the carry bit, denoted by *CARRY*, calculated by **Eq.21**. The third output is the borrowing bit, denoted by *BORROW*, calculated by **Eq.22**. The fourth and fifth outputs are garbage outputs. **Figure 4** shows the block diagram of the reversible binary half adder and subtractor.

$$SUM = A \oplus B \quad \textbf{Eq. 20}$$

$$CARRY = (A.B \oplus C) \quad \textbf{Eq. 21}$$

$$BORROW = \overline{(A}.B) \oplus C \quad \textbf{Eq. 22}$$

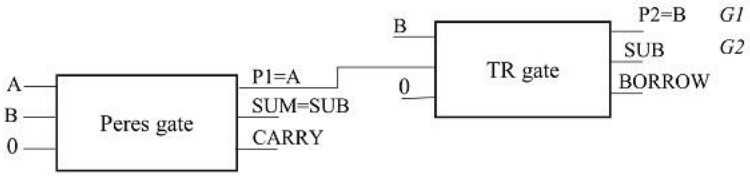


Figure 4: Block diagram of reversible half adder/subtractor

3.2.2 Reversible Binary Full Adder/Subtractor

The full adder/subtractor circuit is used to perform the addition and subtraction of three bits. The reversible binary full adder/subtractor can be built using the reversible Double Peres Gate (DPG), NOT, and Fredkin gates. The Double Peres Gate is used to design the reversible full adder. The NOT and Fredkin gates are used to design the reversible full subtractor.

The reversible binary full adder/subtractor circuit takes 4 bits inputs. The first three inputs (*A, B,* and *C*) are the three bits required to be added or subtracted. The fourth bit (*D*) is a constant bit with a value of zero. The circuit returns five outputs. The first output is the summation bit, denoted by *SUM*. It is also the difference bit, which is calculated by **Eq.23**. The second output is the carry bit, denoted by *CARRY*, which is calculated by **Eq.24**. The third output is the borrowing bit, denoted by *BORROW*, which is calculated by **Eq.25**. Finally, the fourth and fifth outputs are garbage outputs. The block diagram of reversible binary full adder/subtractor is shown in **Figure 5**.

$$SUM = (A \oplus B \oplus C) \quad \textbf{Eq. 23}$$

$$CARRY = (A \oplus B).C \oplus (A.B) \quad \textbf{Eq. 24}$$

$$BORROW = \overline{(A \oplus B)}.C) \oplus (A \oplus B).\bar{A} \quad \textbf{Eq. 25}$$

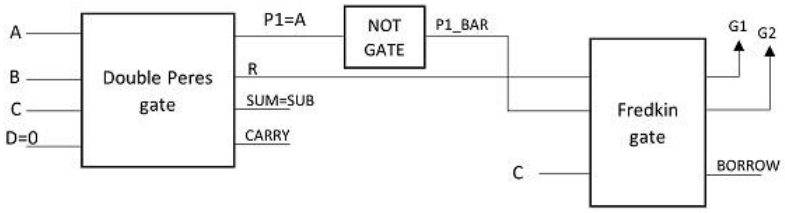


Figure 5: Block diagram of reversible full adder/subtractor

4. Result and Discussion

This section presents the results of the reversible binary half and full adder/subtractor and a comparison between the proposed design and existing designs in terms of gate count, constant input, garbage output, and quantum cost.

The reversible half and full adder/subtractor circuits are simulated and verified using the Xilinx ISE 14.7 simulator. In addition, the circuits are synthesized using the Verilog, a Hardware Description Language (HDL). Furthermore, the waveforms are generated to verify the performance of both proposed designs. **Figure 6** shows the waveform results of the reversible half adder/subtractor. The variables a, b and c are the inputs and p1, p2, sum, sub, carry, and borrow are the output variables. The waveform conforms to the desired working of the reversible half adder/subtractor circuit. Likewise, **Figure 7** shows the waveform of the reversible full adder and subtractor. The variables a, b, cin, and d are the inputs and sum_sub, carry, borrow, p1, p1_bar, r, q1 and g2 are the output variables.

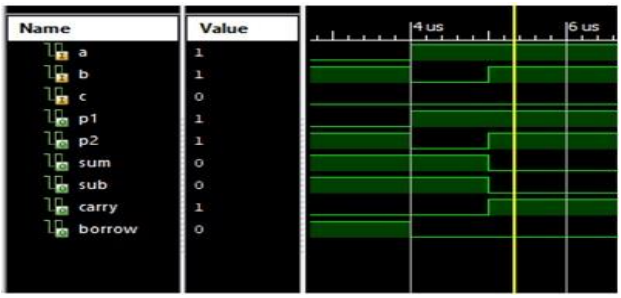


Figure 6: Waveform of reversible binary half adder/subtractor

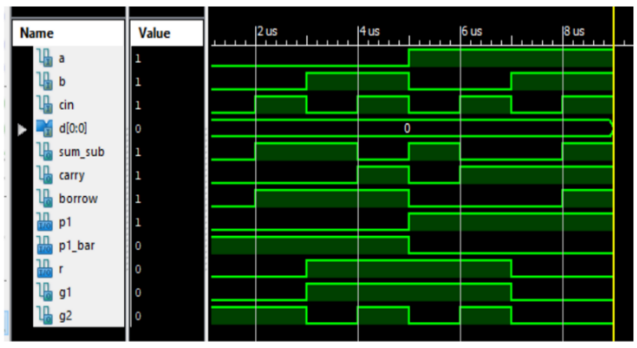


Figure 7: Waveform of reversible binary full adder/subtractor

The comparisons of the proposed reversible half and full adder/subtractor and other designs are made in terms of the number of gates, constant bits, garbage bits, and the quantum cost. The comparison of the proposed reversible half adder and subtractor and other designs is shown in **Table 2**. Meanwhile, the comparison of the proposed reversible full adder and subtractor with other designs is shown in **Table 3**.

Table 2: Comparison of different designs of half adder/subtractor

Reference	Gate Out	Garbage Output	Constant Input	Quantum Cost
Proposed design	2	2	1	6
[14]	4	3	2	10
[9]	3	0	3	8
[15]	1	0	2	6
[16]	1	Not reported	2	Not reported

As shown in **Table 2**, the proposed half adder/subtractor achieves the lowest quantum cost of six, similar with work [15]. Although work in [15] obtain lower gate count and zero garbage output, but it only operates as a half subtractor.

Table 3: Comparison of different designs of full adder/subtractor

Reference	Gate Out	Garbage Output	Constant Input	Quantum Cost
Proposed design	3	2	1	9
[14]	4	4	4	11
[9]	1 block	3	1	14
[15]	2	2	2	Not reported
[16]	Two half adder/subtractor	5	1	22

As depicted in **Table 3**, the full adder/subtractor design proposed in this work achieve the lowest quantum cost of nine. It also has minimum number of garbage output and constant input.

5. Conclusion

In this paper, reversible binary half and full adder/subtractor designs are presented. Both designs are built using basic reversible logic gates. The circuit is designed and synthesized using Verilog. The performance comparison results for both reversible half and full adder/subtractor show that the proposed designs achieve the lowest number of quantum cost. In addition, the reversible adder/subtractor also efficient in terms of the number of gates, number of garbage output and number of constant bits when compared to other existing designs. The advancement and development of synthesis and designing can lead to improving the existing designs. Some possible future work is investigating a new methodology and a new reversible gate to build a floating adder.

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